



# **Application Note**

**EON EN25Q80A**

**VS**

**Winbond W25Q80BV**

## **Specification Comparison**



## 1. INTRODUCTION

The application note introduces how to implement a system design from Winbond W25Q80BV Flash to Eon EN25Q80A Flash.

## 2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q80A	W25Q80BV
<b>Voltage Range</b>	2.7 ~ 3.6	2.7 ~ 3.6
<b>Pin to Pin Compatible (Quad mode)</b>	8-pins SOP 150mil / 208mil 8 contact VDFN (5x6mm) 8-pin DIP	8-pin SOP 150mil / 208mil 8-Pad WSON (5x6mm) 8-Pin DIP
<b>SPI frequency (standard / dual / quad mode)</b>	100MHz / 80MHz / 80MHz	100MHz / 80MHz / 80MHz
<b>Secured Silicon Sector Region</b>	256 Byte	64 Bit (8 Byte) Unique Serial Number 4 x 256 Byte Security Register
<b>Sector Architecture</b>	Uniform 256 Sectors of 4 K byte 16 blocks of 64 K byte	Uniform 256 sectors of 4 K byte 16 blocks of 64 K byte 32 blocks of 32 K byte
<b>SPI mode</b>	Mode 0 / Mode 3	Mode 0 / Mode 3
<b>Minimum Endurance Cycle</b>	100K	100K
<b>Package</b>	8-pins SOP 150mil / 208mil 8 contact VDFN (5x6mm) 8-pin DIP	8-pin SOP 150mil / 208mil 8-Pad WSON (5x6mm) 8-Pin DIP



## 3. HARDWARE CONSIDERATIONS

### 3.1 I<sub>CC</sub> comparison

Current	EN25Q80A	W25Q80BV	Unit
	Max	Max	
Read I <sub>CC3</sub>	25	18	mA
Page Program (PP) I <sub>CC4</sub>	28	25	mA
Sector Erase (SE) I <sub>CC6</sub>	25	25	mA
Standby I <sub>CC1</sub>	20	50	μA

### 3.2 Pin Configuration

Pin number	EN25Q80A	W25Q80BV
Pin1	CS#	CS#
Pin2	DO (DQ1)	DO (IO1)
Pin3	WP# (DQ2)	WP# (IO2)
Pin4	VSS	VSS
Pin5	DI (DQ0)	DI (IO0)
Pin6	CLK	CLK
Pin7	NC (DQ3)	HOLD# (IO3)
Pin8	VCC	VCC

**Note:**

For the pin Configuration of 8 pin SOP and VDFN (5x6mm) package, Eon EN25Q80A Flash is the same as Winbond W25Q80BV Flash when using Quad Mode function only.



## 4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

### For EN25Q80A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			13h
90h	1Ch		13h
9Fh	1Ch	3014h	

### For W25Q80BV

<b>MANUFACTURER ID</b>	<b>(MF7-MF0)</b>	
Winbond Serial Flash	EFh	
<b>Device ID</b>	<b>(ID7-ID0)</b>	<b>(ID15-ID0)</b>
<b>Instruction</b>	<b>ABh, 90h, 92h, 94h</b>	<b>9Fh</b>
W25Q80BV	13h	4014h



## 4.2. Instruction Set Comparison

### 4.2.1 Enable Quad I/O (EQIO) command (38h)

EN25Q80A : Support.

W25Q80BV : No support.

### 4.2.2 Reset Quad I/O (RSTQIO) command (FFh)

EN25Q80A : Support.

W25Q80BV : No support.

### 4.2.3 Write Enable for Volatile Status Register command

EN25Q80A : No support.

W25Q80BV : Support.

### 4.2.4 Different Read Status Register command

EN25Q80A : Only support 05h command. (for register bit 7~ bit0)

W25Q80BV : Support 05h (for register bit 7~ bit 0) and 35h. (for register bit 8 ~ bit 15)

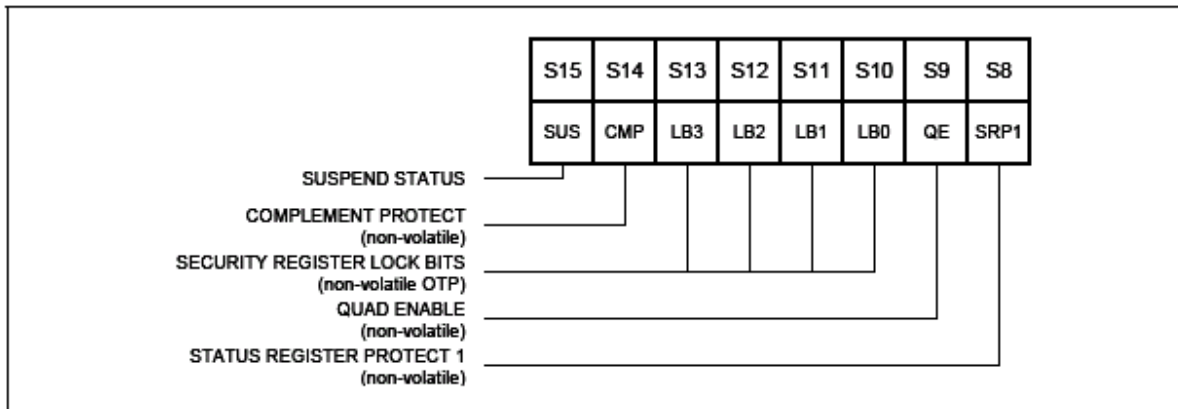
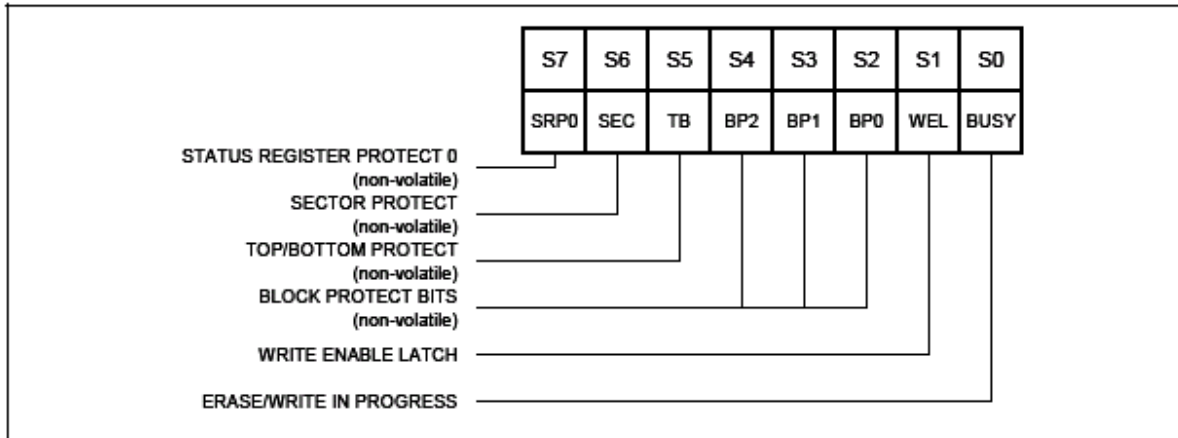
### 4.2.5 Different Read Status Register length

EN25Q80A : 8 bit. (bit7 ~ bit 0)

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable		(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit



**W25Q80BV : 16 bit. (Bit 15 ~ bit0)**



#### 4.2.6 Quad page program command

**EN25Q80A : No support.**

**W25Q80BV : Support.**

#### 4.2.7 Different block erase command

**EN25Q80A : Only support D8h command. (for 64K byte)**

**W25Q80BV : Support 52h (for 32K byte) and D8h commands. (for 64K Byte)**

#### 4.2.8 Erase / Program suspend commands

**EN25Q80A : No support.**

**W25Q80BV : Support.**

#### 4.2.9 Erase / Program resume commands

**EN25Q80A : No support.**

**W25Q80BV : Support.**



## 4.2.10 Continue read mode reset commands (for Dual / Quad operation)

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.11 Fast read quad output command

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.12 Word read for quad I/O command

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.13 Octal word read for quad I/O command

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.14 Set Burst with wrap

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.15 Manufacture/Device ID by Dual/Quad I/O command

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.16 Read Unique ID command

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.17 Erase/Program/Read Security Registers command

EN25Q80A : No support.

W25Q80BV : Support.

## 4.2.18 Enter OTP mode command (3Ah)

EN25Q80A : Support.

W25Q80BV : No support.



## 4.2.19 Different block protect definition

EN25Q80A :

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 253	000000h-0FDFFFh	1016KB	Lower 254/256
0	1	0	Sector 0 to 251	000000h-0FBFFFh	1008KB	Lower 252/256
0	1	1	Sector 0 to 247	000000h-0F7FFFh	992KB	Lower 248/256
1	0	0	Sector 0 to 239	000000h-0EFFFFh	960KB	Lower 240/256
1	0	1	Sector 0 to 223	000000h-0DFFFFh	896KB	Lower 224/256
1	1	0	Sector 0 to 191	000000h-0BFFFFh	768KB	Lower 192/256
1	1	1	All	000000h-0FFFFFFh	1024KB	All

W25Q80BV :

Status Register Memory Protection (CMP = 0)

STATUS REGISTER <sup>(1)</sup>					W25Q80BV (8M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	15	0F0000h – 0FFFFFFh	64KB	Upper 1/16
0	0	0	1	0	14 and 15	0E0000h – 0FFFFFFh	128KB	Upper 1/8
0	0	0	1	1	12 thru 15	0C0000h – 0FFFFFFh	256KB	Upper 1/4
0	0	1	0	0	8 thru 15	080000h – 0FFFFFFh	512KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/16
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/8
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/4
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/2
0	X	1	0	1	0 thru 15	000000h – 0FFFFFFh	1MB	ALL
X	X	1	1	X	0 thru 15	000000h – 0FFFFFFh	1MB	ALL
1	0	0	0	1	15	0FF000h – 0FFFFFFh	4KB	Top Block
1	0	0	1	0	15	0FE000h – 0FFFFFFh	8KB	Top Block
1	0	0	1	1	15	0FC000h – 0FFFFFFh	16KB	Top Block
1	0	1	0	X	15	0F8000h – 0FFFFFFh	32KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	X	0	000000h – 007FFFh	32KB	Bottom Block



# Eon Silicon Solution Inc.

## Status Register Memory Protection (CMP = 1)

STATUS REGISTER <sup>(1)</sup>					W25Q80BV (8M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 15	000000h – 0FFFFFFh	1MB	ALL
0	0	0	0	1	0 thru 14	000000h – 0EFFFFh	960KB	Lower 15/16
0	0	0	1	0	0 thru 13	000000h – 0DFFFFh	896KB	Lower 7/8
0	0	0	1	1	0 thru 11	000000h – 0BFFFFh	768KB	Lower 3/4
0	0	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/2
0	1	0	0	1	1 thru 15	010000h – 0FFFFFFh	960KB	Upper 15/16
0	1	0	1	0	2 thru 15	020000h – 0FFFFFFh	896KB	Upper 7/8
0	1	0	1	1	4 thru 15	040000h – 0FFFFFFh	768KB	Upper 3/4
0	1	1	0	0	8 thru 15	080000h – 0FFFFFFh	512KB	Upper 1/2
0	X	1	0	1	NONE	NONE	NONE	NONE
X	X	1	1	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 14	000000h – 0FEFFFFh	1,020KB	Lower 255/256
1	0	0	1	0	0 thru 14	000000h – 0FDFFFFh	1,016KB	Lower 127/128
1	0	0	1	1	0 thru 14	000000h – 0FBFFFFh	1,008KB	Lower 63/64
1	0	1	0	X	0 thru 14	000000h – 0F7FFFFh	992KB	Lower 31/32
1	1	0	0	1	1 thru 15	001000h – 0FFFFFFh	1,020KB	Upper 255/256
1	1	0	1	0	1 thru 15	002000h – 0FFFFFFh	1,016KB	Upper 127/128
1	1	0	1	1	1 thru 15	004000h – 0FFFFFFh	1,008KB	Upper 63/64
1	1	1	0	X	1 thru 15	008000h – 0FFFFFFh	992KB	Upper 31/32



## 5. PERFORMANCE DIFFERENCES

### 5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q80A		W25Q80BV		Unit
	Typ	Max	Typ	Max	
4 KB Sector Erase Time	0.09	0.3	0.03	0.2	sec
64KB Block Erase Time	0.5	2	0.15	1	sec
Chip (Bulk) Erase Time	8	20	2	6	sec
Page Programming Time	1.3	5	0.7	3	ms

### 5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q80A	W25Q80BV
tCH (serial clock high time)	Min @ 4ns	Min @ 4ns
tCL (serial clock low time)	Min @ 4ns	Min @ 4ns
tCLCH(serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCHCL(serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tSLCH(CS# active setup time)	Min@ 5ns	Min @ 5ns
tCHSH(CS# active hold time)	Min@ 5ns	Min @ 5ns
tSHSL(CS# high time)	Min @ 15ns for Read Min @ 50ns for Write	Min @ 10ns for Read Min @ 50ns for Write
tDSU(Data in setup time)	Min @ 2ns	Min @ 2ns
tDH(Data in hold time)	Min @ 5ns	Min @ 5ns



# Eon Silicon Solution Inc.

---

---

## Revisions List

Revision No	Description	Date
A	Initial Release	2009/12/15