



# **Application Note**

**EON EN25Q80A**

**VS**

**SST SST25VF080B**

## **Specification Comparison**



# Eon Silicon Solution Inc.

## 1. INTRODUCTION

The application note introduces how to implement a system design from SST SST25VF080B Flash to Eon EN25Q80A Flash.

## 2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q80A	SST25VF080B
Voltage Range	2.7 ~ 3.6	2.7 ~ 3.6
Pin to Pin Compatible (Quad mode)	8-pins SOP 150mil / 208mil 8 contact VDFN (5x6mm) 8-pin DIP	8-pin SOP 208mil 8-Pad WSON (5x6mm) 8-Pin DIP
SPI frequency (standard / dual / quad mode)	100MHz (standard mode) 80MHz @ dual & quad mode	50MHz @ standard mode
Secured Silicon Sector Region	256 Byte	No
Sector Architecture	Uniform 256 Sectors of 4 K byte 16 blocks of 64 K byte	Uniform 256 sectors of 4 K byte 16 blocks of 64 K byte 32 blocks of 32 K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
Minimum Endurance Cycle	100K	100K
Package	8-pins SOP 150mil / 208mil 8 contact VDFN (5x6mm) 8-pin DIP	8-pin SOP 208mil 8-Pad WSON (5x6mm) 8-Pin DIP



## 3. HARDWARE CONSIDERATIONS

### 3.1 I<sub>CC</sub> comparison

Current	EN25Q80A	SST25VF080B	Unit
	Max	Max	
Read I <sub>CC3</sub>	25 @ 100MHz 20 @ 80MHz	18 @ 50MHz	mA
Page Program (PP) I <sub>CC4</sub>	28	30	mA
Sector Erase (SE) I <sub>CC6</sub> Block Erase (BE) I <sub>CC7</sub>	25	30	mA
Standby I <sub>CC1</sub>	20	20	μA

### 3.2 Pin Configuration

Pin number	EN25Q80A	SST25VF080B
Pin1	CS#	CE#
Pin2	DO (DQ1)	SO
Pin3	WP# (DQ2)	WP#
Pin4	VSS	VSS
Pin5	DI (DQ0)	SI
Pin6	CLK	CLK
Pin7	NC (DQ3)	HOLD#
Pin8	VCC	VDD

**Note:**

1. If customers don't use HOLD# pin function on SST25VF080B, which can be replaced by EN25Q80A in standard SPI mode.
2. SST25VF080B can support general standard SPI mode.
3. EN25Q80A can support general standard / dual / quad SPI mode.  
(Need specific SPI controller)



## 4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

### For EN25Q80A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			13h
90h	1Ch		13h
9Fh	1Ch	3014h	

### For SST25VF080B

OP code: 9Fh

Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
BFH	25H	8EH

OP code: 90h or ABh

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID SST25VF080B	00001H	8EH



## 4.2. Instruction Set Comparison

### 4.2.1 Different Read Status Register content

**EN25Q80A :**

**S5 is reserved bit, S6 is WPDIS bit, S7 are SRP bit and OTP\_LOCK bit (in OTP mode).**

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable		(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

**SST25VF080B :**

**Bit 0 is BP3, Bit 6 is AAI and Bit 7 is BPL.**

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection	1	R/W
3	BP1	Indicate current level of block write protection	1	R/W
4	BP2	Indicate current level of block write protection	1	R/W
5	BP3	Indicate current level of block write protection	0	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W



## 4.2.2 Different block protect area definitions of (BP0~BP3)

**EN25Q80A :**

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 253	000000h-0FDFFFh	1016KB	Lower 254/256
0	1	0	Sector 0 to 251	000000h-0FBFFFh	1008KB	Lower 252/256
0	1	1	Sector 0 to 247	000000h-0F7FFFh	992KB	Lower 248/256
1	0	0	Sector 0 to 239	000000h-0EFFFFh	960KB	Lower 240/256
1	0	1	Sector 0 to 223	000000h-0DFFFFh	896KB	Lower 224/256
1	1	0	Sector 0 to 191	000000h-0BFFFFh	768KB	Lower 192/256
1	1	1	All	000000h-0FFFFFFh	1024KB	All

**SST25VF080B :**

Protection Level	Status Register Bit <sup>2</sup>				Protected Memory Address
	BP3	BP2	BP1	BP0	8 Mbit
None	X	0	0	0	None
Upper 1/16	X	0	0	1	F0000H-FFFFFFH
Upper 1/8	X	0	1	0	E0000H-FFFFFFH
Upper 1/4	X	0	1	1	C0000H-FFFFFFH
Upper 1/2	X	1	0	0	80000H-FFFFFFH
All Blocks	X	1	0	1	00000H-FFFFFFH
All Blocks	X	1	1	0	00000H-FFFFFFH
All Blocks	X	1	1	1	00000H-FFFFFFH

1. X = Don't Care (RESERVED) default is '0'

2. Default at power-up for BP2, BP1, and BP0 is '111'. (All Blocks Protected)

## 4.2.3 Enable Quad I/O (EQIO) (38h) command

**EN25Q80A : Support.**

**SST25VF080B : No support.**

## 4.2.4 Reset Quad I/O (RSTQIO) (FFh) command

**EN25Q80A : Support.**

**SST25VF080B : No support.**



## 4.2.5 Different block erase command

**EN25Q80A** : Only support D8h command. (for 64K byte)

**SST25VF080B** : Support 52h (for 32K byte) and D8h commands. (for 64K Byte)

## 4.2.6 Dual Output FAST\_READ (3Bh) commands

**EN25Q80A** : Support.

**SST25VF080B** : No support.

## 4.2.7 Dual Input / Output FAST\_READ (BBh) commands

**EN25Q80A** : Support.

**SST25VF080B** : No support.

## 4.2.8 Quad Input / Output FAST\_READ (EBh) commands

**EN25Q80A** : Support.

**SST25VF080B** : No support.

## 4.2.9 Enter OTP Mode (3Ah) commands

**EN25Q80A** : Support.

### OTP Sector Address

Sector	Sector Size	Address Range
255	256 byte	0FF000h – 0FF0FFh

Note: The OTP sector is mapping to sector 255

**SST25VF080B** : No support.

## 4.2.10 Auto Address Increment Programming commands

**EN25Q80A** : No support.

**SST25VF080B** : Support.

## 4.2.11 Enable Write Status Register commands

**EN25Q80A** : No support.

**SST25VF080B** : Support.



## 4.2.12 Enable SO to output RY/BY# status during AAI programming commands

EN25Q80A : No support.

SST25VF080B : Support.

## 4.2.13 Disable SO to output RY/BY# status during AAI programming commands

EN25Q80A : No support.

SST25VF080B : Support.

## 5. PERFORMANCE DIFFERENCES

### 5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q80A		SST25VF080B		Unit
	Typ	Max	Typ	Max	
Page Programming Time	1.3	5	1.8	2.56	ms
4 KB Sector Erase Time	0.09	0.3	-	0.025	sec
64KB Block Erase Time	0.5	2	0.018	0.025	sec
Chip (Bulk) Erase Time	8	20	0.035	0.05	sec

### 5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q80A	SST25VF080B
tCH (serial clock high time)	Min @ 4ns	Min @ 9ns
tCL (serial clock low time)	Min @ 4ns	Min @ 9ns
tCLCH(serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCLCL(serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tSLCH(CS# active setup time)	Min@ 5ns	Min @ 5ns
tCHSH(CS# active hold time)	Min@ 5ns	Min @ 5ns
tSHSL(CS# high time)	Min @ 15ns for Read Min @ 50ns for Write	Min @ 50ns
tDSU(Data in setup time)	Min @ 2ns	Min @ 2ns
tDH(Data in hold time)	Min @ 5ns	Min @ 5ns



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## Revisions List

Revision No	Description	Date
A	Initial Release	2009/12/15