



Application Note

**Eon Flash EN29GL064H/L/T/B
VS
MXIC Flash MX29GL640E/H/L/T/B**



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from MXIC MX29GL640E/H/L/T/B Flash to Eon EN29GL064H/L/T/B Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

The following table highlights the major features of these two devices.

Features	EN29GL064H/L/T/B	MX29GL640E/H/L/T/B
voltage range	2.7 ~ 3.6	2.7 ~ 3.6
Pin to Pin	Compatible (for 48 / 56 TSOP) Compatible (for 64 FBGA)	Compatible (for 48 / 56 TSOP) Compatible (for 64 FBGA)
Page Access time	25ns	25ns
Random access time	70ns	90ns
Read buffer length	16 Byte	16 Byte
Write buffer length	32 Byte	32 Byte
Sector Architecture	Uniform 64K Byte @ H / L 8 x 8K Byte boot sectors + 127 x 64K Byte sector @ T / B	Uniform 64K Byte @H / L 8 x 8K Byte boot sectors + 127 x 64K Byte sector @T / B
Byte/Word mode	Yes	Yes
Secured silicon sector	256 Byte	256 Byte
CFI Compliant	Yes	Yes
JEDEC Data# polling & toggle bit command	Yes	Yes
Erase Suspend / Resume	Yes	Yes
Program Suspend / Resume	Yes	Yes
Minimum endurance cycle	100K	100K
Package	48-pin 12mm x 20mm TSOP 56-pin 14mm x 20mm TSOP 64-ball 11mm x 13mm FBGA	48-pin 12mm x 20mm TSOP 56-pin 14mm x 20mm TSOP 64 ball 11mm x 13mm FBGA

Note:

EN29GL064H: The highest address sector protected when WP#/ACC = "L".

EN29GL064L: The Lowest address sector protected when WP#/ACC = "L".

EN29GL064T: Top boot sector

EN29GL064B: Bottom boot sector.



3. HARDWARE & PERFORMANCE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN29GL064H/L/T/B		MX29GL640E/H/L/T/B		Unit
	Typ	Max	Typ	Max	
Read I _{CC1} (@5MHz)	15	30	30	50	mA
Write I _{CC2}	20	30	26	30	mA
Standby I _{CC3}	1.5	10	30	100	μA

3.2 Max VID comparison

MX29GL640E/H/L/T/B VID range is 9.5V ~ 10.5V. But EN29GL064H/L/T/B doesn't support VID function. Any voltage level higher than chip spec would damage the device, possibly. (Using high voltage on Address9 enters autoselect mode)

3.3 Different V_{HH} level (for accelerating programming functions)

EN29GL064H/L/T/B voltage level: 8.5V ~ 9.5V.

MX29GL640E/H/L/T/B voltage level: 9.5 ~ 10.5V.

3.4 Different V_{IO} level (for adjusting different I/O voltage range)

EN29GL064H/L/T/B voltage level: 1.65V ~ 3.6V.

MX29GL640E/H/L/T/B voltage level: 2.7V ~ 3.6V.

3.5 Different random access speed

EN29GL064H/L/T/B: 70ns @ full VCC range: 2.7V ~ 3.6V.

MX29GL640E/H/L/T/B: 90ns @ full VCC range: 2.7V ~ 3.6V.



4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer ID, Device Identifications comparison

Eon		MXIC	
Manufacture ID: 007Fh (A8 = "0"), 001Ch (A8 = "1").		Manufacture ID: 00C2h	
Part No.	Device ID	Part No.	Device ID
EN29GL064H (Uniform, highest address sector protected)	227Eh / 220Ch / 2201h	MX29GL640EH (Uniform, highest address sector protected)	227Eh / 220Ch / 2201h
EN29GL064L (Uniform, lowest address sector protected)	227Eh / 220Ch / 2201h	MX29GL640EL (Uniform, lowest address sector protected)	227Eh / 220Ch / 2201h
EN29GL064T (Top boot)	227Eh / 2210h / 2201h	MX29GL640ET (Top boot)	227Eh / 2210h / 2201h
EN29GL064B (Bottom Boot)	227Eh / 2210h / 2200h	MX29GL640EB (Bottom Boot)	227Eh / 2210h / 2200h

4.2. Password protection commands

EN29GL064H/L/T/B: No support.

MX29GL640E/H/L/T/B: Support.

4.3. Multi-sector erasure commands

EN29GL064H/L/T/B: No supported. (Users must issue another sector erase command for the next sector to be erased after the previous one is completed)

MX29GL640E/H/L/T/B: Support.

4.4. Different PPB protect range

EN29GL064H/L: Sector 0~3 and 124~127 have PPB for each sector. Sector 4~123 are 1 PPB per 4 sectors.

EN29GL064T: Sector 0~123 are 1 PPB per 4 sectors. Sector 124~134 have PPB for each boot sector.

EN29GL064B: Sector 0~10 have PPB for each boot sector. Sector 11~134 are 1 PPB per 4 sectors.

MX29GL640EH/L/T/B: A Solid Write Protection Bit (SPB) is assigned to each block.



5. PERFORMANCE DIFFERENCES

5.1 Power-on and Reset Timings.

Parameter	Description	EN29GL064H/L/T/B	MX29GL640E/H/L/T/B
t _{VCS}	Vcc Setup Time (min)	50μs	500us
t _{RP1}	RESET# Pulse Width (During Embedded Algorithms)	10us	10us
t _{RP2}	RESET# Pulse Width (NOT During Embedded Algorithms)	500ns	500ns
t _{RH}	Reset# High Time Before Read	50ns	200ns
t _{RB1}	RY/BY# Recovery Time (to CE#, OE# go low)	0ns	0ns
t _{RB2}	RY/BY# Recovery Time (to WE# go low)	50ns	50ns
t _{READY1}	Reset# Pin Low (During Embedded Algorithms) to Read or Write	20μs	20us
t _{READY2}	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	500ns	500ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2009/07/21
B	Update 4.1 Manufacturer ID, Device Identifications comparison on page 4	2011/02/10