



# **Application Note**

**EON EN25Q32A**

**VS**

**Numonyx M25P32**

## **Specification Comparison**



# Eon Silicon Solution Inc.

## 1. INTRODUCTION

The application note introduces how to implement a system design from Numonyx M25P32 Flash to Eon EN25Q32A Flash.

## 2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q32A	M25P32
Voltage Range	2.7 ~ 3.6	2.7 ~ 3.6
Pin to Pin Compatible (standard SPI mode)	8-pins SOP 200mil 8 contact VDFN Except Vpp and HOLD# pin	SO8W (208mil) VFQFPN8 6 x 5mm (MLP8)
SPI frequency	100MHz (standard mode) 80MHz @ dual & quad mode	75MHz (standard mode)
Secured Silicon Sector Region	512 Byte	N/A
Sector Architecture	Uniform 1024 sectors of 4K byte 64 blocks of 64K byte	Uniform 64 sectors of 64K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
Minimum Endurance Cycle	100K	100K
Package	8-pins SOP 150mil 8-pins SOP 200mil 8 contact VDFN 8-pins DIP	SO16 (300mil) SO8W (208mil) VDFPN8 8 x 6mm (MLP8) VFQFPN8 6 x 5mm (MLP8)



## 3. HARDWARE CONSIDERATIONS

### 3.1 I<sub>CC</sub> comparison

Current	EN25Q32A	M25P32	Unit
	Max	Max	
Read I <sub>CC3</sub>	25 @ 100MHz 20 @ 80MHz	12 @ 75MHz 4 @ 33MHz	mA
Page Program (PP) I <sub>CC4</sub>	28	15	mA
Sector Erase (SE) I <sub>CC6</sub>	25	15	mA
Standby I <sub>CC1</sub>	20	50	μA

### 3.2 Pin Configuration (8-pin package)

Pin number	EN25Q32A	M25P32
Pin1	CS#	S#
Pin2	DO (DQ1)	Q
Pin3	WP# (DQ2)	W# / V <sub>pp</sub>
Pin4	VSS	VSS
Pin5	DI (DQ0)	D
Pin6	CLK	C
Pin7	NC (DQ3)	HOLD#
Pin8	VCC	VCC

#### Note:

1. Eon EN25Q32A Flash can support the general standard / dual / quad SPI mode (Need specific SPI controller), but don't support the V<sub>pp</sub> pin (V<sub>pp</sub> = 9 V for Fast Program/Erase mode) and HOLD# pin functions.
2. For the general standard / SPI mode, Eon EN25Q32A Flash is the same as NUMONYX M25P32 Flash if customer don't use the V<sub>pp</sub> pin and HOLD# pin functions.
3. NUMONYX M25P32 doesn't support the dual and quad SPI modes.



## 4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

### For EN25Q32A

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			15h
90h	1Ch		15h
9Fh	1Ch	3016h	

### For M25P32

Manufacturer identification	Device identification		UID	CFI content
	Memory type	Memory capacity		
20h	20h	16h	10h	16 bytes



## 4.2. Instruction Set Comparison

### 4.2.1 Different Block Protection Area

#### EN25Q32A :

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 62	000000h-3EFFFFh	4032KB	Lower 63/64
0	0	1	0	Block 0 to 61	000000h-3DFFFFh	3968KB	Lower 62/64
0	0	1	1	Block 0 to 59	000000h-3BFFFFh	3840KB	Lower 60/64
0	1	0	0	Block 0 to 55	000000h-37FFFFh	3584KB	Lower 56/64
0	1	0	1	Block 0 to 47	000000h-2FFFFFFh	3072KB	Lower 48/64
0	1	1	0	Block 0 to 31	000000h-1FFFFFFh	2048KB	Lower 32/64
0	1	1	1	All	000000h-3FFFFFFh	4096KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 63 to 1	3FFFFFFh-010000h	4032KB	Upper 63/64
1	0	1	0	Block 63 to 2	3FFFFFFh-020000h	3968KB	Upper 62/64
1	0	1	1	Block 63 to 4	3FFFFFFh-040000h	3840KB	Upper 60/64
1	1	0	0	Block 63 to 8	3FFFFFFh-080000h	3584KB	Upper 56/64
1	1	0	1	Block 63 to 16	3FFFFFFh-100000h	3072KB	Upper 48/64
1	1	1	0	Block 63 to 32	3FFFFFFh-200000h	2048KB	Upper 32/64
1	1	1	1	All	000000h-3FFFFFFh	4096KB	All

#### M25P32 :

Status Register content			Memory content	
BP2 bit	BP1 bit	BP0 bit	Protected area	Unprotected area
0	0	0	none	All sectors <sup>(1)</sup> (64 sectors: 0 to 63)
0	0	1	Upper 64th (Sector 63)	Lower 63/64ths (63 sectors: 0 to 62)
0	1	0	Upper 32nd (two sectors: 62 and 63)	Lower 31/32nds (62 sectors: 0 to 61)
0	1	1	Upper sixteenth (four sectors: 60 to 63)	Lower 15/16ths (60 sectors: 0 to 59)
1	0	0	Upper eighth (eight sectors: 56 to 63)	Lower seven-eighths (56 sectors: 0 to 55)
1	0	1	Upper quarter (sixteen sectors: 48 to 63)	Lower three-quarters (48 sectors: 0 to 47)
1	1	0	Upper half (thirty-two sectors: 32 to 63)	Lower half (32 sectors: 0 to 31)
1	1	1	All sectors (64 sectors: 0 to 63)	none

1. The device is ready to accept a Bulk Erase instruction only if, all Block Protect (BP2, BP1, BP0) are 0.



## 4.2.2 Different RDSR bit definition

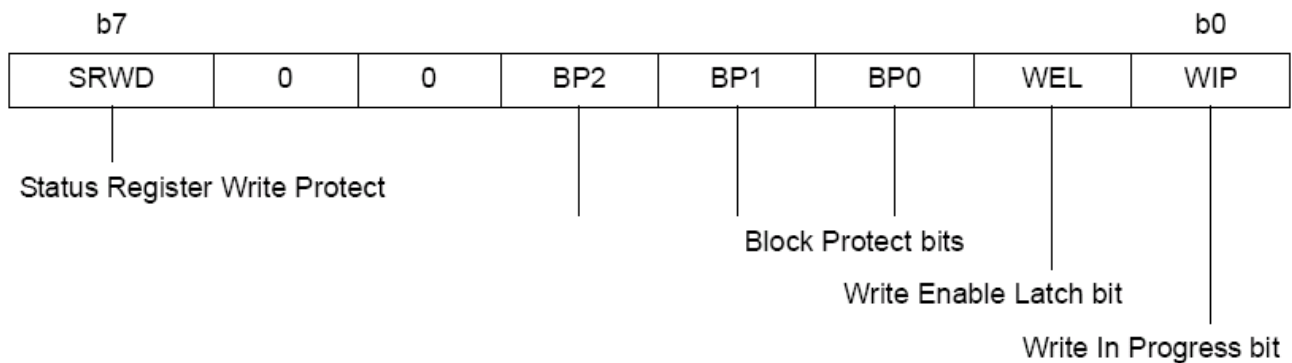
### EN25Q32A :

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

**Note**

1. In OTP mode, SRP bit is served as OTP\_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

### M25P32 :





## 4.2.6 Dual I/O Fast Read command

EN25Q32A: Support. (BBh)

M25P32 : No Support.

## 4.2.7 Quad I/O Fast Read command

EN25Q32A: Support. (EBh)

M25P32 : No Support.

## 4.2.8 Different Sector Erase command

EN25Q32A: 20h (for 4KB small sector use)

M25P32: D8h (for 64KB sector use, the same with EN25Q32A Block Erase commands)

## 4.2.9 Read Manufacturer / Device ID command

EN25Q32A: Support. (90h)

M25P32 : No Support.

## 4.2.10 Enter Secured OTP command

EN25Q32A: Support. (3Ah)

M25P32 : No Support.

## 4.2.11 Exit Secured OTP command

EN25Q32A: Support. (04h)

M25P32 : No Support.

## 4.2.12 Secured OTP Addresses

EN25Q32A:

Sector	Sector Size	Address Range
1023	512 byte	3FF000h – 3FF1FFh

Note: The OTP sector is mapping to sector 1023

M25P32 : No Support.



## 5. PERFORMANCE DIFFERENCES

### 5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q32A		M25P32		Unit
	Typ	Max	Typ	Max	
Sector Erase Time (4KB size @ EN25Q32A) (64KB size @ M25P32)	0.09	0.3	0.6	3	sec
Block Erase Time	0.5	2	N/A	N/A	sec
Chip (Bulk) Erase Time	25	50	23	80	sec
Page Programming Time	1.3	5	0.64	5	ms

### 5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q32A	M25P32
tCH (serial clock high time)	Min @ 4ns	Min @ 6ns
tCL (serial clock low time)	Min @ 4ns	Min @ 6ns
tCLCH(serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCLCL(serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCHSH(CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
tSHSL(CS# high time)	Min, read @15ns Program/Erase @50ns	Min @ 100ns
tDSU(Data in setup time)	Min @ 2ns	Min @ 2ns
tDH(Data in hold time)	Min @ 5ns	Min @ 5ns



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## Revisions List

Revision No	Description	Date
A	Initial Release	2010/02/02