



Application Note

EON EN25Q40

VS

Numonyx M25P40

Specification Comparison



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from Numonyx M25P40 Flash to Eon EN25Q40 Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN25Q40	M25P40
Voltage Range	2.7 ~ 3.6	2.7 ~ 3.6
Pin to Pin Compatible (standard SPI mode)	8-pins SOP 150mil 8 contact VDFN Except Vpp and HOLD# pin	SO8 (150mil) VFQFPN8 6 x 5mm (MLP8)
SPI frequency	100MHz (standard mode) 80MHz @ dual & quad mode	75MHz (standard mode)
Secured Silicon Sector Region	256 Byte	N/A
Sector Architecture	Uniform 128 sectors of 4K byte 8 blocks of 64K byte	Uniform 8 sectors of 64K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
Minimum Endurance Cycle	100K	100K
Package	8-pins SOP 150mil 8 contact VDFN	SO8 (150mil) SO8W (208mil) VFQFPN8 6 x 5mm (MLP8) QFN8L 6 x 5mm (MLP8)



3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN25Q40	M25P40	Unit
	Max	Max	
Read I _{CC3}	25 @ 100MHz 20 @ 80MHz	8 @ 75MHz 4 @ 33MHz	mA
Page Program (PP) I _{CC4}	28	15	mA
Sector Erase (SE) I _{CC6}	25	15	mA
Standby I _{CC1}	20	100	μA

3.2 Pin Configuration (8-pin package)

Pin number	EN25Q40	M25P40
Pin1	CS#	S#
Pin2	DO (DQ1)	Q
Pin3	WP# (DQ2)	W#
Pin4	VSS	VSS
Pin5	DI (DQ0)	D
Pin6	CLK	C
Pin7	NC (DQ3)	HOLD#
Pin8	VCC	VCC

Note:

1. Eon EN25Q40 Flash can support the general standard / dual / quad SPI mode (Need specific SPI controller), but don't support the HOLD# pin functions.
2. For the general standard / SPI mode, Eon EN25Q40 Flash is the same as NUMONYX M25P40 Flash if customer don't use the HOLD# pin functions.
3. NUMONYX M25P40 doesn't support the dual and quad SPI modes.



4. SOFTWARE CONSIDERATIONS

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

For EN25Q40

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			12h
90h	1Ch		12h
9Fh	1Ch	3013h	

For M25P40

Manufacturer identification	Device identification		UID	
	Memory type	Memory capacity	CFD length	CFD content
20h	20h	13h	10h	16 bytes



4.2. Instruction Set Comparison

4.2.1 Different Block Protection Area

EN25Q40 :

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 125	000000h-07DFFFh	504KB	Lower 126/128
0	1	0	Sector 0 to 123	000000h-07BFFFh	496KB	Lower 124/128
0	1	1	Sector 0 to 119	000000h-077FFFh	480KB	Lower 120/128
1	0	0	Sector 0 to 111	000000h-06FFFFh	448KB	Lower 112/128
1	0	1	Sector 0 to 95	000000h-05FFFFh	384KB	Lower 96/128
1	1	0	Sector 0 to 63	000000h-03FFFFh	256KB	Lower 64/128
1	1	1	All	000000h-07FFFFh	512KB	All

M25P40 :

Status Register content			Memory content	
BP2 bit	BP1 bit	BP0 bit	Protected area	Unprotected area
0	0	0	none	All sectors ⁽¹⁾ (eight sectors: 0 to 7)
0	0	1	Upper eighth (Sector 7)	Lower seven-eighths (seven sectors: 0 to 6)
0	1	0	Upper quarter (two sectors: 6 and 7)	Lower three-quarters (six sectors: 0 to 5)
0	1	1	Upper half (four sectors: 4 to 7)	Lower half (four sectors: 0 to 3)
1	0	0	All sectors (eight sectors: 0 to 7)	none
1	0	1	All sectors (eight sectors: 0 to 7)	none
1	1	0	All sectors (eight sectors: 0 to 7)	none
1	1	1	All sectors (eight sectors: 0 to 7)	none

1. The device is ready to accept a Bulk Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) are 0.



4.2.2 Different RDSR bit definition

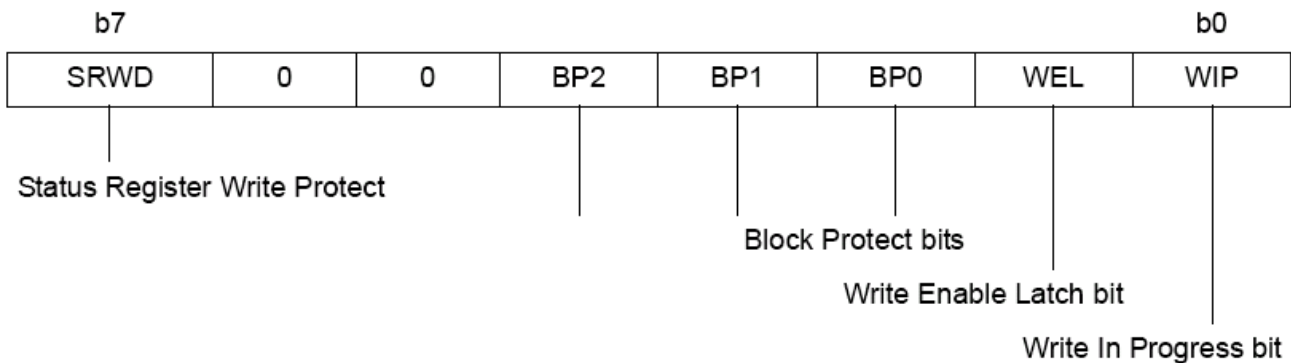
EN25Q40 :

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable		(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

M25P40 :



4.2.3 Enable Quad I/O (EQIO) command

EN25Q40: Support. (38h)

M25P40 : No Support.

4.2.4 Reset Quad I/O (RSTQIO) command

EN25Q40: Support. (FFh)

M25P40 : No Support.

4.2.5 Dual Output Fast Read command

EN25Q40: Support. (3Bh)

M25P40 : No Support.

4.2.6 Dual I/O Fast Read command

EN25Q40: Support. (BBh)

M25P40 : No Support.



4.2.7 Quad I/O Fast Read command

EN25Q40: Support. (EBh)

M25P40 : No Support.

4.2.8 Different Sector Erase command

EN25Q40: 20h (for 4KB small sector use)

M25P40: D8h (for 64KB sector use, the same with EN25Q40 Block Erase commands)

4.2.9 Read Manufacturer / Device ID command

EN25Q40: Support. (90h)

M25P40 : No Support.

4.2.10 Enter Secured OTP command

EN25Q40: Support. (3Ah)

M25P40 : No Support.

4.2.11 Exit Secured OTP command

EN25Q40: Support. (04h)

M25P40 : No Support.

4.2.12 Secured OTP Addresses

EN25Q40:

Sector	Sector Size	Address Range
127	256 byte	07F000h – 07F0FFh

Note: The OTP sector is mapping to sector 127

M25P40 : No Support.



5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q40		M25P40		Unit
	Typ	Max	Typ	Max	
Sector Erase Time (4KB size @ EN25Q40) (64KB size @ M25P40)	0.09	0.3	1	3	sec
Block Erase Time	0.5	2	N/A	N/A	sec
Chip (Bulk) Erase Time	3.5	10	4.5	10	sec
Page Programming Time	1.3	5	1.4	5	ms

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q40	M25P40
tCH (serial clock high time)	Min @ 4ns	Min @ 6ns
tCL (serial clock low time)	Min @ 4ns	Min @ 6ns
tCLCH(serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCLCL(serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
tCHSH(CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
tSHSL(CS# high time)	Min, read @15ns Program/Erase @50ns	Min @ 100ns
tDSU(Data in setup time)	Min @ 2ns	Min @ 2ns
tDH(Data in hold time)	Min @ 5ns	Min @ 5ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2010/02/02