



Migration Note

EON Flash EN25B64 to EN25Q64



Eon Silicon Solution Inc.

1. INTRODUCTION

The application note introduces how to implement a system design from EON EN25B64 Flash to Eon EN25Q64 Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table is major features of these two devices.

Features	EN25Q64	EN25B64
Voltage range	2.7 ~ 3.6	2.7 ~ 3.6
Pin to Pin Compatible (standard SPI mode)	16-pin SOP 300mil Except pin 1 = NC	16-pin SOP 300mil Except pin 1 = HOLD#
SPI frequency	104MHz (standard mode) 80MHz @ dual & quad mode	100MHz (standard mode)
Secured Silicon Sector region	512 Byte	512 Byte
Sector Architecture	Uniform 2048 sectors of 4K byte 128 blocks of 64K byte	Flexible Sector 2 sectors of 4K byte 1 sectors of 8K byte 1 sectors of 16K byte 1 sectors of 32K byte 127 sectors of 64K byte
SPI mode	Mode 0 / Mode 3	Mode 0 / Mode 3
EQIO mode (Full Quad mode)	Yes	No
Reset-Enable / Reset	Yes	No
Dual Output Fast Read	Yes	No
Dual I/O Fast Read	Yes	No
Quad I/O Fast Read	Yes	No
Page program	Yes	Yes
Sector Erase 4K byte	Yes	No
Block (Sector) Erase 64K byte	Yes	Yes
BP table	Enhanced protect (Note)	Conventional
Minimum endurance cycle	100K	100K
Package	8-pin SOP 200mil 8 contact VDFN (5x6mm) 8 contact VDFN (6x8mm) 8-pin PDIP 16-pin SOP 300mil 24 balls BGA (6x8mm)	16-pin SOP 300mil

Note: Please refer to page 5



3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

Current	EN25Q64	EN25B64	Unit
	Max	Max	
Read I _{CC3}	25 @ 104MHz 20 @ 80MHz	20 @ 100MHz	mA
Page Program (PP) I _{CC4}	28	15	mA
Sector Erase (SE) I _{CC6}	25	15	mA
Standby I _{CC1}	20	20	μA

3.2 The following table is pin comparison (16-pin SOP 300mil)

Pin number	EN25Q64	EN25B64
Pin 1	NC (DQ3)	HOLD#
Pin 2	VCC	VCC
Pin 3	NC	NC
Pin 4	NC	NC
Pin 5	NC	NC
Pin 6	NC	NC
Pin 7	CS#	CS#
Pin 8	DO (DQ1)	DO
Pin 9	WP# (DQ2)	WP#
Pin 10	VSS	VSS
Pin 11	NC	NC
Pin 12	NC	NC
Pin 13	NC	NC
Pin 14	NC	NC
Pin 15	DI (DQ0)	DI
Pin 16	CLK	CLK

Note:

If customers don't use Hold# pin function on EN25B64, which can be replaced by EN25Q64 in standard SPI mode.

EN25B64 only support general standard SPI mode.

EN25Q64 can support general standard / dual / quad SPI mode. (Need specific SPI controller)



4. SOFTWARE CONSIDERATIONS

Except of memory type, (only difference on 9Fh command) there is no difference in Manufacture ID, Device ID

4.1 Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density)

For EN25Q64

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			16h
90h	1Ch		16h
9Fh	1Ch	3017h	

For EN25B64

Boot Type	OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
EN25B64(Bottom Boot)	ABh			36h
	90h	1Ch		36h
	9Fh	1Ch	2017h	
EN25B64T(Top Boot)	ABh			46h
	90h	1Ch		46h
	9Fh	1Ch	2017h	



4.2 Instruction Set Comparison

4.2.1 Different Block Protection Area

EN25Q64 :

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 126	000000h-7EFFFFh	8128KB	Lower 127/128
0	0	1	0	Block 0 to 125	000000h-7DFFFFh	8064KB	Lower 126/128
0	0	1	1	Block 0 to 123	000000h-7BFFFFh	7936KB	Lower 124/128
0	1	0	0	Block 0 to 119	000000h-77FFFFh	7680KB	Lower 120/128
0	1	0	1	Block 0 to 111	000000h-6FFFFFFh	7168KB	Lower 112/128
0	1	1	0	Block 0 to 95	000000h-5FFFFFFh	6144KB	Lower 96/128
0	1	1	1	All	000000h-7FFFFFFh	8192KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 127 to 1	7FFFFFFh-010000h	8128KB	Upper 127/128
1	0	1	0	Block 127 to 2	7FFFFFFh-020000h	8064KB	Upper 126/128
1	0	1	1	Block 127 to 4	7FFFFFFh-040000h	7936KB	Upper 124/128
1	1	0	0	Block 127 to 8	7FFFFFFh-080000h	7680KB	Upper 120/128
1	1	0	1	Block 127 to 16	7FFFFFFh-100000h	7168KB	Upper 112/128
1	1	1	0	Block 127 to 32	7FFFFFFh-200000h	6144KB	Upper 96/128
1	1	1	1	All	7FFFFFFh-000000h	8192KB	All

EN25B64 :

Protected Area Sizes- Bottom Boot Sector Organization

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Sectors	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0	000000h-000FFFh	4KB	Lower 1/2048
0	1	0	Sector 0 to 1	000000h-001FFFh	8KB	Lower 1/1024
0	1	1	Sector 0 to 2	000000h-003FFFh	16KB	Lower 1/512
1	0	0	Sector 0 to 3	000000h-007FFFh	32KB	Lower 1/256
1	0	1	Sector 0 to 4	000000h-00FFFFh	64KB	Lower 1/128
1	1	0	Sector 0 to 67	000000h-3FFFFFFh	4096KB	Lower 1/2
1	1	1	All	000000h-7FFFFFFh	8192KB	All



Protected Area Sizes- Top Boot Sector Organization

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Sectors	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 131	7FF000h-7FFFFFFh	4KB	Upper 1/2048
0	1	0	Sector 130 to 131	7FE000h-7FFFFFFh	8KB	Upper 1/1024
0	1	1	Sector 129 to 131	7FC000h-7FFFFFFh	16KB	Upper 1/512
1	0	0	Sector 128 to 131	7F8000h-7FFFFFFh	32KB	Upper 1/256
1	0	1	Sector 127 to 131	7F0000h-7FFFFFFh	64KB	Upper 1/128
1	1	0	Sector 64 to 131	400000h-7FFFFFFh	4096KB	Upper 1/2
1	1	1	All	000000h-7FFFFFFh	8192KB	All

4.2.2 Different RDSR bit definition

EN25Q64 :

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit) (Note 3)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

EN25B64 :

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	Reserved bits	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected			(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit				Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".



4.2.3 Secured OTP Addresses

EN25Q64 :

Sector	Sector Size	Address Range
2047	512 byte	7FF000h – 7FF1FFh

Note: The OTP sector is mapping to sector 2047

EN25B64 :

Bottom Boot Security Sector Address

Sector	Sector Size	Address Range
0	512 byte	000000h – 0001FFh

Note: The OTP sector is mapping to sector 0

Top Boot Security Sector Address

Sector	Sector Size	Address Range
131	512 byte	7FFE00h – 7FFFFFFh

Note: The OTP sector is mapping to sector 131

4.3 Erasable

EN25Q64--- Sector, Block or Chip erasable

EN25B64--- Sector or Chip erasable

Note : In the condition of erasing the boot sector of EN25B64 to be replaced with EN25Q64, one or multiple sector erase command (20h) must be issued in EN25Q64 depending on the sector size. The correlation table is shown below.



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Sector Size	Address Range	EN25B64	EN25Q64
4KByte	00000h-00FFFh	Issue sector erase (D8h) for sector 0	Issue sector erase (20h) for sector 0
4KByte	01000h-01FFFh	Issue sector erase (D8h) for sector 1	Issue sector erase (20h) for sector 1
8KByte	02000h-03FFFh	Issue sector erase (D8h) for sector 2	Issue sector erase (20h) for sector 2
			Issue sector erase (20h) for sector 3
16KByte	04000h-07FFFh	Issue sector erase (D8h) for sector 3	Issue sector erase (20h) for sector 4
			Issue sector erase (20h) for sector 5
			Issue sector erase (20h) for sector 6
			Issue sector erase (20h) for sector 7
32KByte	08000h-0FFFFh	Issue sector erase (D8h) for sector 4	Issue sector erase (20h) for sector 8
			.
			Issue sector erase (20h) for sector 15

Note:

EN25B64 is bottom sector, for EN25B64T (top sector) the boot sectors are in high address.

4.4 For EQIO (38h), RSTQIO (FFh), RSTEN (66h), RST (99h), Dual output fast read 3Bh), Dual I/O fast read (BBh) and Quad I/O fast read (EBh) commands are only available on EN25Q64



5. PERFORMANCE DIFFERENCES

5.1 ERASE AND PROGRAM PERFORMANCE

The erasing and programming performance comparison.

Parameter	EN25Q64		EN25B64		Unit
	Typ	Max	Typ	Max	
Page Programming Time	1.3	5	1.5	5	ms
Sector Erase Time (4KB)	0.09	0.3	0.3	0.6	Sec
Sector Erase Time (16KB)	N/A	N/A	0.5	1	Sec
Block / Sector Erase Time (64KB)	0.5	2	0.8	2	Sec
Chip Erase Time	30*	50	50*	80	Sec

*NOTE: ERASE FROM "1" → "1".

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q64	EN25B64
tCH (serial clock high time)	Min@ 4ns	Min@ 4ns
tCL (serial clock low time)	Min@ 4ns	Min@ 4ns
tCLCH(serial clock rise time)	Min@ 0.1V / ns	Min@ 0.1V / ns
tCLCL(serial clock fall time)	Min@ 0.1V / ns	Min@ 0.1V / ns
tCHSH(CS# active setup / hold time)	Min@ 5ns	Min@ 5ns
tSHSL(CS# high time)	Min, read @15ns Program/Erase @50ns	Min@ 50ns
tDSU(Data in setup time)	Min@2ns	Min@2ns
tDH(Data in hold time)	Min@5ns	Min@5ns



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Revisions List

Revision No	Description	Date
A	Initial Release	2010/02/25