Application Note

EON EN29GL256

(Version : F)

vs

MXIC MX29GL256E

(Version : 1.1)

1. INTRODUCTION

The application note introduces how to implement a system design from MXIC MX29GL256E Flash to Eon EN29GL256 Flash.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1 The following table highlights the major features of these two devices.

Features	EN29GL256	MX29GL256E
Voltage range	2.7 ~ 3.6V	2.7 ~ 3.6V
Pin to pin compatible	56-pin TSOP 64-ball BGA (11 x 13 mm)	56-pin TSOP 64-ball LFBGA (11 x 13 mm)
Access time	90ns @ 2.7 ~ 3.6V	100ns @ 2.7 ~ 3.6V 90ns @ 3.0 ~ 3.6V
Secured silicon sector region	256 byte	256 byte
Sector architecture	Uniform 256 sectors of 128K byte	Uniform 256 sectors of 128K byte
Minimum endurance cycle	100K	100K
Package	56-pin TSOP 64-ball BGA (11 x 13 mm)	56-pin TSOP 64-ball FBGA (10 x 13 mm) 64-ball LFBGA (11 x 13 mm) 70-pin SSOP

3. HARDWARE CONSIDERATIONS

3.1 I_{CC} comparison

The I_{CC} performance of EN29GL256 is better than MX29GL256E.

Current	EN29GL256	MX29GL256E	Unit
	Max	Max	
Read I_{CC1}	45	100	mA
Program / Erase I_{CC3}	30	30	mA
Standby I_{CC4}	10	100	µA

3.2 Device operating modes

EN29GL256

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	A0-A23	DQ0-DQ7	DQ8-DQ15	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8-DQ14= High-Z, DQ15 = A-1
Write	L	H	L	H	(Note 1)	A_{IN}	D_{IN}	D_{IN}	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	D_{IN}	D_{IN}	
CMOS Standby	V_{CC} ±0.3V	X	X	V_{CC}±0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z

Notes:
1. Addresses are A23:A0 in word mode; A23:A-1 in byte mode.
2. If WP# = VIL, on the outermost sector remains protected. If WP# = VIH, the outermost sector is unprotected. WP# has an internal pull-up; when unconnected, WP# is at VIH. All sectors are unprotected when shipped from the factory (The Secured Silicon Sector can be factory protected depending on version ordered.)
3. DIN or DOUT as required by command sequence, data polling, or sector protect algorithm.

Legend
L = Logic Low = VIL, H = Logic High = VIH, VHH = 8.5–9.5V, X = Don't Care, AIN = Address In, DIN = Data In, DOUT = Data Out

EN29GL256 does not support Sector Lock Status Verification, Read Manufacturer ID, and Read Device ID in autoselect mode.

Mode Select	RE-SET#	CE#	WE#	OE#	Address (Note4)	Data I/O Q0~Q7	Byte# Vil Data (I/O) Q8~Q15	Byte# Vih Data (I/O) Q8~Q15	WP#/ ACC
Device Reset	L	X	X	X	X	HighZ	HighZ	HighZ	L/H
Standby Mode	Vcc ± 0.3V	Vcc± 0.3V	X	X	X	HighZ	HighZ	HighZ	H
Output Disable	H	L	H	H	X	HighZ	HighZ	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	Q8-Q14= HighZ, Q15=A-1	DOUT	L/H
Write	H	L	L	H	AIN	DIN		DIN	Note1,2
Accelerate Program	H	L	L	H	AIN	DIN		DIN	Vhv

Notes:
1. The first or last sector was protected if WP#/ACC=Vil.
2. When WP#/ACC = Vih, the protection conditions of the outmost sector depends on previous protection conditions. Refer to the advanced protect feature.
3. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
4. In Word Mode (Byte#=Vih), the addresses are AM to A0, AM: MSB of address.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15), AM: MSB of address.

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q0 ~ Q7	Q8 ~ Q15
	CE#	WE#	OE#											
Sector Lock Status Verification	L	H	L	SA	X	V_{hv}	X	L	X	L	H	L	01h or 00h (Note 1)	X
Read Silicon ID Manufacturer Code	L	H	L	X	X	V_{hv}	X	L	X	L	L	L	C2H	X
Read Silicon ID – MX29GL256E														
Cycle 1	L	H	L	X	X	V_{hv}	X	L	X	L	L	H	7EH	22H(Word), XXH(Byte)
Cycle 2	L	H	L	X	X	V_{hv}	X	L	X	H	H	L	22H	22H(Word), XXH(Byte)
Cycle 3	L	H	L	X	X	V_{hv}	X	L	X	H	H	H	01H	22H(Word), XXH(Byte)

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: WP# protects high address sector: 99h.
   WP# protects low address sector: 89h
   Factory unlocked code: WP# protects high address sector: 19h.
   WP# protects low address sector: 09h
3. AM: MSB of address.

4. SOFTWARE CONSIDERATIONS

4.1. Instruction set comparison

EN29GL256

The manufacturer ID and Device ID of EN29GL256 and MX29GL256E are different.

For Read Lock Register instruction, the address of 1st cycle of EN29GL256 is 00 while that of MX29GL256E is don't care.

Command Sequence			Cycles	Bus Cycles											
				1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	XXX	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F				
										100	1C				
		Byte		AAA		555		AAA		000	7F				
										200	1C				
	Device ID	Word	4	555	AA	2AA	55	555	90	X01	227E	X0E	2222	X0F	2201
		Byte		AAA		555		AAA		X02	7E	X1C	22	X1E	01
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA) X02	00				
											01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Write to Buffer		Word	6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
		Byte		AAA		555									
Program Buffer to Flash		Word	1	SA	29										
		Byte													
Write to Buffer Abort Reset		Word	3	555	AA	2AA	55	555	F0						
		Byte		AAA		555		AAA							
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase/Program Suspend			1	XXX	B0										
Erase/Program Resume			1	XXX	30										
Secured Silicon Sector Entry			3	555	AA	2AA	55	555	88						
Secured Silicon Sector Exit			4	555	AA	2AA	55	555	90	XX	00				
CFI Query		Word	1	55	98										
		Byte		AA											
Accelerated Program			2	XX	A0	PA	PD								

Legend
X = Don't care
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same write buffer page as PA.
WC = Word Count is the number of write buffer locations to load minus 1 and maximum value is 31 for word and byte mode.

Command Sequence			Cycles	Bus Cycles											
				1st. Cycle		2nd. Cycle		3rd. Cycle		4th. Cycle		5th. Cycle		6th. Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register	Command Set Entry	Word	3	555	AA	2AA	55	555	40						
		Byte	3	AAA	AA	55	55	AAA	40						
	Program		2	XXX	A0	XXX	Data								
	Read		1	00	RD										
	Command Set Exit		2	XXX	90	XXX	00								
Global Non-Volatile	PPB Command Set Entry	Word	3	555	AA	2AA	55	555	C0						
		Byte	3	AAA	AA	55	55	AAA	C0						
	PPB Program		2	XXX	A0	SA	00								
	All PPB Erase		2	XXX	80	00	30								
	PPB Status Read		1	SA	RD										
	PPB Command Set Exit		2	XXX	90	XXX	00								
Global Volatile Freeze	PPB Lock Command Set Entry	Word	3	555	AA	2AA	55	555	50						
		Byte	3	AAA	AA	555	55	AAA	50						
	PPB Lock Set		2	XXX	A0	XXX	00								
	PPB Lock Status Read		1	XXX	RD										
	PPB Lock Command Set Exit		2	XXX	90	XXX	00								
Volatile	DYB Command Set Entry	Word	3	555	AA	2AA	55	555	E0						
		Byte	3	AAA	AA	555	55	AAA	E0						
	DYB Set		2	XXX	A0	SA	00								
	DYB Clear		2	XXX	A0	SA	01								
	DYB Status Read		1	SA	RD										
	DYB Command Set Exit		2	XXX	90	XXX	00								

Legend
X = Don't care
RD(0) = Read data.
SA = Sector Address. Address bits Amax–A16 uniquely select any sector.
PWD = Password
PWDx = Password word0, word1, word2, and word3.
Data = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit,
PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

MX29GL256E

EN29GL256 does not support Factory Protect Verify, Deep power down, and Password Protection.

Comm-and		Read Mode	Reset Mode	Automatic Select								Security Sector Region		Exit Security Sector	
				Silicon ID		Device ID		Factory Protect Verify		Sector Protect Verify					
				Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cycle	Addr	Addr	XXX	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	555	2AA	555	2AA	555	2AA	555	2AA	555	2AA	555
	Data			55	55	55	55	55	55	55	55	55	55	55	55
3rd Bus Cycle	Addr			555	AAA	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
	Data			90	90	90	90	90	90	90	90	88	88	90	90
4th Bus Cycle	Addr			X00	X00	X01	X02	X03	X06	(Sector) X02	(Sector) X04			XXX	XXX
	Data			C2h	C2h	ID1	ID1	99/19(H) 89/09(L)		00/01	00/01			00	00
5th Bus Cycle	Addr					X0E	X1C								
	Data					ID2	ID2								
6th Bus Cycle	Addr					X0F	X1E								
	Data					ID3	ID3								

Comm-and		Program		Write to Buffer Program		Write to Buffer Program Abort Reset		Write to Buffer Program confirm		Chip Erase		Sector Erase		CFI Read		Program/ Erase Suspend		Program/ Erase Resume	
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cycle	Addr	555	AAA	555	AAA	555	AAA	SA	SA	555	AAA	555	AAA	55	AA	xxx	xxx	xxx	xxx
	Data	AA	AA	AA	AA	AA	AA	29	29	AA	AA	AA	AA	98	98	B0	B0	30	30
2nd Bus Cycle	Addr	2AA	555	2AA	555	2AA	555			2AA	555	2AA	555						
	Data	55	55	55	55	55	55			55	55	55	55						
3rd Bus Cycle	Addr	555	AAA	SA	SA	555	AAA			555	AAA	555	AAA						
	Data	A0	A0	25	25	F0	F0			80	80	80	80						
4th Bus Cycle	Addr	Addr	Addr	SA	SA					555	AAA	555	AAA						
	Data	Data	Data	N-1	N-1					AA	AA	AA	AA						
5th Bus Cycle	Addr			WA	WA					2AA	555	2AA	555						
	Data			WD	WD					55	55	55	55						
6th Bus Cycle	Addr			WBL	WBL					555	AAA	Sec-tor	Sec-tor						
	Data			WD	WD					10	10	30	30						

WA= Write Address
WD= Write Data
SA= Sector Address
N-1= Word Count
WBL= Write Buffer Location
PWD= Password
PWDn=Password word 0, word 1, word n
ID1/ID2/ID3: Refer to Table 2-2 for detail ID.

Command		Deep Power Down				Password Protection									
		Enter		Exit		Password Command Set Entry		Password Program		Password Read		Password Unlock		Password Command Set Exit	
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cycle	Addr	555	AAA	XXX	XXX	555	AAA	XXX	XXX	X00	X00	00	00	XXX	XXX
	Data	AA	AA	AB	AB	AA	AA	A0	A0	PWD0	PWD0	25	25	90	90
2nd Bus Cycle	Addr	2AA	555			2AA	555	PWA	PWA	X01	X01	00	00	XXX	XXX
	Data	55	55			55	55	PWD	PWD	PWD1	PWD1	03	03	00	00
3rd Bus Cycle	Addr	XXX	XXX			555	AAA			X02	X02	X00	X00		
	Data	B9	B9			60	60			PWD2	PWD2	PWD0	PWD0		
4th Bus Cycle	Addr									X03	X03	X01	X01		
	Data									PWD3	PWD3	PWD1	PWD1		
5th Bus Cycle	Addr										X04	X02	X02		
	Data										PWD4	PWD2	PWD2		
6th Bus Cycle	Addr										X05	X03	X03		
	Data										PWD5	PWD3	PWD3		
7th Bus Cycle	Addr										X06	00	X04		
	Data										PWD6	29	PWD4		
8th Bus Cycle	Addr										X07		X05		
	Data										PWD7		PWD5		
9th Bus Cycle	Addr												X06		
	Data												PWD6		
10th Bus Cycle	Addr												X07		
	Data												PWD7		
11th Bus Cycle	Addr												00		
	Data												29		

Command		Lock Register								Global Non-Volatile							
		Lock register Command Set Entry		Program		Read		Lock register Command Set Exit		SPB Command Set Entry		SPB Program		All SPB Erase		SPB Status Read	
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cycle	Addr	555	AAA	XXX	XXX	XXX	XXX	XXX	XXX	555	AAA	XXX	XXX	XXX	XXX	SA	SA
	Data	AA	AA	A0	A0	DATA	DATA	90	90	AA	AA	A0	A0	80	80	00/01	00/01
2nd Bus Cycle	Addr	2AA	555	XXX	XXX			XXX	XXX	2AA	555	SA	SA	00	00		
	Data	55	55	Data	Data			00	00	55	55	00	00	30	30		
3rd Bus Cycle	Addr	555	AAA							555	AAA						
	Data	40	40							C0	C0						
4th Bus Cycle	Addr																
	Data																
5th Bus Cycle	Addr																
	Data																

Command		Global Non-Volatile		Global Volatile Freeze								Volatile					
		SPB Command Set Exit		SPB Lock Command Set Entry		SPB Lock Set		SPB Lock Status Read		SPB Lock Command Set Exit		DPB Command Set Entry		DPB Set		DPB Clear	
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cycle	Addr	XXX	XXX	555	AAA	XXX	XXX	XXX	XXX	XXX	XXX	555	AAA	XXX	XXX	XXX	XXX
	Data	90	90	AA	AA	A0	A0	00/01	00/01	90	90	AA	AA	A0	A0	A0	A0
2nd Bus Cycle	Addr	XXX	XXX	2AA	555	XXX	XXX			XXX	XXX	2AA	555	SA	SA	SA	SA
	Data	00	00	55	55	00	00			00	00	55	55	00	00	01	01
3rd Bus Cycle	Addr			555	AAA							555	AAA				
	Data			50	50							E0	E0				
4th Bus Cycle	Addr																
	Data																
5th Bus Cycle	Addr																
	Data																

Command		Volatile			
		DPB Status Read		DPB Command Set Exit	
		Word	Byte	Word	Byte
1st Bus Cycle	Addr	SA	SA	XXX	XXX
	Data	00/01	00/01	90	90
2nd Bus Cycle	Addr			XXX	XXX
	Data			00	00
3rd Bus Cycle	Addr				
	Data				
4th Bus Cycle	Addr				
	Data				
5th Bus Cycle	Addr				
	Data				

Notes:

* It is not recommended to adopt any other code not in the command definition table which will potentially enter the hidden mode.
* For the SPB Lock and DPB Status Read "00" means lock (protect), "01" means unlock (unprotect).

4.3 Different sector protection bits combination

The combination of sector protection bits are different.

EN29GL256

Unique Device PPB Lock Bit 0 = locked 1 = unlocked		Sector PPB 0 = protected 1 = unprotected	Sector DYB 0 = protected 1 = unprotected	Sector Protection Status
Any Sector	0	0	x	Protected through PPB
Any Sector	0	0	x	Protected through PPB
Any Sector	0	1	1	Unprotected
Any Sector	0	1	0	Protected through DYB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	1	0	Protected through DYB
Any Sector	1	1	1	Unprotected

MX29GL256E

Protection Bit Status				Sector Status
DPB	SPBLK	SPB	USPB	
clear	clear	clear	clear	unprotect, DPB/SPB/USPB are changeable
clear	clear	clear	set	unprotect, DPB/SPB/USPB are changeable
clear	clear	set	clear	protect, DPB/SPB/USPB are changeable
clear	clear	set	set	unprotect, DPB/SPB/USPB are changeable
clear	set	clear	clear	unprotect, DPB/USPB are changeable
clear	set	clear	set	unprotect, DPB/USPB are changeable
clear	set	set	clear	protect, DPB/USPB are changeable
clear	set	set	set	unprotect, DPB/USPB are changeable
set	clear	clear	clear	protect, DPB/SPB/USPB are changeable
set	clear	clear	set	protect, DPB/SPB/USPB are changeable
set	clear	set	clear	protect, DPB/SPB/USPB are changeable
set	clear	set	set	protect, DPB/SPB/USPB are changeable
set	set	clear	clear	protect, DPB/USPB are changeable
set	set	clear	set	protect, DPB/USPB are changeable
set	set	set	clear	protect, DPB/USPB are changeable
set	set	set	set	protect, DPB/USPB are changeable

4.4 Different Lock Register bit definition

The definition of Lock Register bits are different except for DQ0 and DQ1.

EN29GL256

DQ15-5	DQ4	DQ3	DQ2	DQ1	DQ0
Reserved	DYB Lock Boot Bit	PPB One Time Programmable Bit	Reserved	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit
(default = 1)	0 = protected all DYB after boot-up 1 = unprotected all DYB after boot-up (default = 1)	0 = All PPB Erase Command disabled 1 = All PPB Erase Command enabled (default = 1)	(default = 1)	0 = Persistent Protection enabled (default = 0)	0 = protected 1 = unprotect (default = 1)

Notes:
1. After the Lock Register Bits Command Set Entry command sequence is written, reads and writes for all Sector are disabled, while reads from other sectors are allowed until exiting this mode.
2. Only DQ0 could be change by Lock Register Bits Command for user. Others bits were set by Factory.

After selecting a sector protection method, each sector can operate in any of the following three states:
1. Constantly locked: The selected sectors are protected and can not be reprogrammed unless PPB lock bit is cleared via hardware reset, or power cycle.
2. Dynamically locked: The selected sectors are protected and can be altered via software commands.
3. Unlocked: The sectors are unprotected and can be erased and/or programmed.

MX29GL256E

Q15-Q3	Q2	Q1	Q0
Don't care	Password Protection Mode Lock Bit	Solid Protection Mode Lock Bit	Secured Silicon Sector Protection Bit

5. PERFORMANCE DIFFERENCES

The erasing and programming performance of EN29GL256 is better than MX29GL256E except for T_{OE} and T_{DS}.

5.1 ERASE AND PROGRAM PERFORMANCE

Parameter		EN29GL256		MX29GL256E		Unit
		Typ	Max	Typ	Max	
Sector erase time		0.1	2	0.6	5	sec
Chip erase time		60	240	128	300	sec
Byte programming time		8	200	N/A	N/A	us
Word programming time		8	200	11	360	us
Chip programming time	Byte	268.8	806.4	100	350	sec
	Word	134.4	403.2			
Total write buffer time		160		200		us
ACC total write buffer time		60		100		us

5.2 KEY AC PARAMETER PERFORMANCE

Parameter	EN29GL256	MX29GL256E
T_{ACC} (address to output delay)	Max @ 90ns	Max @ 110ns
T_{CE} (chip enable to output delay)	Max @ 90ns	Max @ 110ns
T_{PACC} (page access time)	Max @ 25ns	Max @ 30ns
T_{OE} (output enable to output delay)	Max @ 35ns	Max @ 30ns
T_{AS} (address setup time)	Min @ 0ns	Min @ 0ns
T_{DS} (data setup time)	Min @ 40ns	Min @ 30ns
T_{VCS} (Vcc setup time)	Min @ 50us	Min @ 500us

Revisions List

Revision No	Description	Date
A	Initial Release	2010/07/12