



Application Note

EON EN25Q32B (Version: Preliminary 0.2)

VS.

MXIC MX25L3255D (Version: 0.03)



1. INTRODUCTION

The application note introduces how to implement a system design from MXIC flash MX25L3255D to Eon flash EN25Q32B.

2. GENERAL FUNCTION COMPARISON TABLE:

2.1. The following table highlights the major features of these two devices.

Features	EN25Q32B	MX25L3255D
Voltage Range	2.7V ~ 3.6V	2.7V ~ 3.6V
Pin to Pin Compatible	Yes	Yes
SPI Mode	Mode 0 / Mode 3	Mode 0 / Mode 3
SPI Frequency	104MHz (standard mode) 80MHz @ dual & quad mode	104MHz (standard mode) 75MHz @ dual & quad mode
Sector Architecture	Uniform <ul style="list-style-type: none">● 1024 sectors of 4Kbyte● 64 blocks of 64Kbyte● Any sector or block can be erased individually.	Uniform <ul style="list-style-type: none">● 1024 sectors of 4Kbyte● 64 blocks of 64Kbyte● Any sector or block can be erased individually.
Lockable OTP Security Sector	512 Bytes	512 Bytes
Permanent Lock	No	Yes
Read Protection	No	Yes
Minimum Endurance Cycle	100K	100K
Package ¹ .	8 pins SOP 200mil body width 8 contact VDFN 16 pins SOP 300mil body width 24 balls BGA (6x8mm) <ul style="list-style-type: none">● All Pb-free packages are RoHS compliant	8 pins SOP 200mil body width 24 balls BGA (6x8mm) <ul style="list-style-type: none">● All Pb-free packages are RoHS compliant

Note:

1. Please refer to the datasheet in detail.



3. HARDWARE CONSIDERATIONS

3.1. I_{CC} Comparison

Current	EN25Q32B	MX25L3255D	Unit
	Max (@ Single 104MHz)	Max (@ Single 104MHz)	
Read I _{CC3}	25	25	mA
Page Program (PP) I _{CC4}	28	20	mA
Sector Erase (SE) I _{CC6}	25	20	mA
Standby I _{CC1}	20	20	μA

3.2. Pins Description

EN25Q32B		MX25L3255D	
Pin Name	Function	Pin Name	Function
CLK	Serial Clock Input	SCLK	Serial Clock Input
DI (DQ0)	Serial Data Input (Data Input Output 0) *1	SI (SIO0)	Serial Data Input (Data Input Output 0) *1
DO (DQ1)	Serial Data Output (Data Input Output 1) *1	SO (SIO1)	Serial Data Output (Data Input Output 1) *1
CS#	Chip Enable	CS#	Chip Enable
WP# (DQ2)	Write Protect (Data Input Output 2) *2	WP# (SIO2)	Write Protect (Data Input Output 2) *2
NC(DQ3)	Not Connect (Data Input Output 3) *2	NC(SIO3)	Not Connect (Data Input Output 3) *2
Vcc	Supply Voltage (2.7-3.6V)	Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground	Vss	Ground
NC	No Connect	NC	No Connect

Note:

1. DQ0 and DQ1 are used for Dual and Quad instructions.
2. DQ0 ~ DQ3 are used for Quad instructions.



4. SOFTWARE CONSIDERATIONS

4.1. Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

4.1.1. For **EN25Q32B** : MANUFACTURER/DEVICE ID TABLE

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			15h
90h	1Ch		15h
9Fh	1Ch	3016h	

4.1.2. For **MX25L3255D** : MANUFACTURER/DEVICE ID TABLE

ID Definitions

RDID Command	manufacturer ID	memory type	memory density
	C2	9E	16
RES Command	electronic ID		
	9E		
REMS/REMS2/REMS4/ Command	manufacturer ID	device ID	
	C2	9E	



4.2. Instruction Set Comparison

4.2.1. For **EN25Q32B** : Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
RSTEN	66h						
RST ⁽¹⁾	99h						
EQIO	38h						
RSTQIO ⁽²⁾	FFh						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0) ⁽³⁾					continuous ⁽⁴⁾
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(5)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(6)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(7)		
Enter OTP mode	3Ah						

Notes:

1. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
2. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode
3. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “()” indicate data being read from the device on the DO pin.
4. The Status Register contents will repeat continuously until CS# terminates the instruction.
5. The Device ID will repeat continuously until CS# terminates the instruction.
6. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction.
00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
7. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.



Instruction Set (Read Instruction)

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) (1)	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh	A23-A8(2)	A7-A0, dummy (2)	(D7-D0, ...) (1)			(one byte per 4 clocks, continuous)
Quad I/O Fast Read	EBh	A23-A0, dummy (4)	(dummy, D7-D0) (5)	(D7-D0, ...) (3)			(one byte per 2 clocks, continuous)

Notes:

1. Dual Output data

$$DQ_0 = (D6, D4, D2, D0)$$

$$DQ_1 = (D7, D5, D3, D1)$$

2. Dual Input Address

$$DQ0 = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, \text{dummy } 6, \text{dummy } 4, \text{dummy } 2, \text{dummy } 0$$

$$DQ1 = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, \text{dummy } 7, \text{dummy } 5, \text{dummy } 3, \text{dummy } 1$$

3. Quad Data

$$DQ0 = (D4, D0, \dots)$$

$$DQ1 = (D5, D1, \dots)$$

$$DQ2 = (D6, D2, \dots)$$

$$DQ3 = (D7, D3, \dots)$$

4. Quad Input Address

$$DQ0 = A20, A16, A12, A8, A4, A0, \text{dummy } 4, \text{dummy } 0$$

$$DQ1 = A21, A17, A13, A9, A5, A1, \text{dummy } 5, \text{dummy } 1$$

$$DQ2 = A22, A18, A14, A10, A6, A2, \text{dummy } 6, \text{dummy } 2$$

$$DQ3 = A23, A19, A15, A11, A7, A3, \text{dummy } 7, \text{dummy } 3$$

5. Quad I/O Fast Read Data

$$DQ0 = (\text{dummy } 12, \text{dummy } 8, \text{dummy } 4, \text{dummy } 0, D4, D0)$$

$$DQ1 = (\text{dummy } 13, \text{dummy } 9, \text{dummy } 5, \text{dummy } 1, D5, D1)$$

$$DQ2 = (\text{dummy } 14, \text{dummy } 10, \text{dummy } 6, \text{dummy } 2, D6, D2)$$

$$DQ3 = (\text{dummy } 15, \text{dummy } 11, \text{dummy } 7, \text{dummy } 3, D7, D3)$$



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4.2.2. For MX25L3255D : Instruction Set

Command Set

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRLB (write read-lock bits2)	BLOCKP (Block Write Lock protection)	PLOCK (Permanent lock)	RDBLOCK (read Block Write Lock status)
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	21 (hex)	E2 (hex)	64 (hex)	FB (hex)
2nd byte						AD1	AD1	AD1
3rd byte						AD2	AD2	AD2
4th byte						AD3	AD3	AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	to write new value of RLB (read-lock bit)	assign a block (64KB) to lock protection	assign a block (64KB) to permanent lock protection	read assigned Block Write Lock status

COMMAND (byte)	RDPLOCK (read permanent lock status)	UNLOCK (chip unprotect)	READ (read data)	FAST READ (fast read data)	2READ (2 x I/O read command) Note1	4READ (4 x I/O read command)	4PP (quad page program)	SE (sector erase)
1st byte	3F (hex)	F3 (hex)	03 (hex)	0B (hex)	BB (hex)	EB (hex)	38 (hex)	20 (hex)
2nd byte	AD1		AD1 (A23-A16)	AD1	ADD(2)	ADD(4) & Dummy(4)	AD1	AD1
3rd byte	AD2		AD2 (A15-A8)	AD2	ADD(2) & Dummy(2)	Dummy(4)		AD2
4th byte	AD3		AD3 (A7-A0)	AD3				AD3
5th byte				Dummy				
Action	read status of permanent lock of block	reset Block Write Lock protection bit whole chip	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	quad input to program the selected page	to erase the selected sector

COMMAND (byte)	BE (block erase)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	AD (hex)	B9 (hex)	AB (hex)	AB (hex)	90 (hex)
2nd byte	AD1		AD1	AD1			x	x
3rd byte	AD2		AD2	AD2			x	x
4th byte	AD3		AD3	AD3			x	ADD (Note 2)
Action	to erase the selected block	to erase whole chip	to program the selected page	continuously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	output the Manufacturer ID & Device ID



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COMMAND (byte)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	Release Read Enhanced	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)
1st byte	EF (hex)	DF (hex)	FFh (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)	70 (hex)	80 (hex)
2nd byte	x	x	x						
3rd byte	x	x	x						
4th byte	ADD (Note 2)	ADD (Note 2)	x						
Action	output the Manufacturer ID & Device ID	output the Manufacturer ID & device ID	All these commands FFh, 00h, AAh or 55h will escape the performance enhance mode	to enter the 4K-bit Secured OTP mode	to exit the 4K-bit Secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO1 which is different from 1 x I/O condition.

Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 3: It is not allowed to adopt any other code which is not in the above command definition table.

Note:

1. The major differences are pointed out by the blue arrows. Please refer to the datasheet in detail.
2. Users must modify the codes for EN25Q32B.



4.3. Different Block Protection Area

4.3.1. For EN25Q32B :

Protected Area Sizes Sector Organization Table

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 0 to 62	000000h-3EFFFFh	4032KB	Lower 63/64
0	0	1	0	Block 0 to 61	000000h-3DFFFFh	3968KB	Lower 62/64
0	0	1	1	Block 0 to 59	000000h-3BFFFFh	3840KB	Lower 60/64
0	1	0	0	Block 0 to 55	000000h-37FFFFh	3584KB	Lower 56/64
0	1	0	1	Block 0 to 47	000000h-2FFFFFFh	3072KB	Lower 48/64
0	1	1	0	Block 0 to 31	000000h-1FFFFFFh	2048KB	Lower 32/64
0	1	1	1	All	000000h-3FFFFFFh	4096KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 63 to 1	3FFFFFFh-010000h	4032KB	Upper 63/64
1	0	1	0	Block 63 to 2	3FFFFFFh-020000h	3968KB	Upper 62/64
1	0	1	1	Block 63 to 4	3FFFFFFh-040000h	3840KB	Upper 60/64
1	1	0	0	Block 63 to 8	3FFFFFFh-080000h	3584KB	Upper 56/64
1	1	0	1	Block 63 to 16	3FFFFFFh-100000h	3072KB	Upper 48/64
1	1	1	0	Block 63 to 32	3FFFFFFh-200000h	2048KB	Upper 32/64
1	1	1	1	All	000000h-3FFFFFFh	4096KB	All

4.3.2. For MX25L3255D :

I. Block Write Lock protection

- The Software Protected Mode (SPM) use A23-A16 address bits to allow a block (64K Byte) of memory to be protected as read only through the Block Write Lock protection command (BLOCKP). This feature allows user to unprotect the entire chip through the chip unprotect command (UNLOCK).



4.4. Different RDSR Bits Definition

The definition of RDSR bits [S7:S2] are different.

4.4.1. For EN25Q32B :

Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit) (Note 3)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit.	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".
3. When executed the (RDSR) (05h) command, the WIP (S0) value is the same as WIP (S7) in table "Suspend Status Register Bit Locations".

4.4.2. For MX25L3255D :

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	x	x	WEL (write enable latch)	WIP (write in progress bit)
reserved	reserved	reserved	reserved	reserved	reserved	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit



4.5. Different One Time Programming Definition

4.5.1. For EN25Q32B :

OTP Sector Address

Sector	Sector Size	Address Range
1023	512 byte	3FF000h – 3FF1FFh

Note: The OTP sector is mapping to sector 1023

4.5.2. For MX25L3255D :

4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	



5. PERFORMANCE DIFFERENCES

5.1. KEY AC PARAMETER PERFORMANCE

Parameter	EN25Q32B	MX25L3255D
t _{CH} (serial clock high time)	Min @ 4ns	Min @ 4.7ns
t _{CL} (serial clock low time)	Min @ 4ns	Min @ 4.7ns
t _{CLCH} (serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t _{CLCL} (serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t _{CHSH} (CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
t _{SLSL} (CS# high time)	Min @ 50ns	Min @ 50ns
t _{DSU} (Data in setup time)	Min @ 2ns	Min @ 2ns
t _{DH} (Data in hold time)	Min @ 5ns	Min @ 5ns

5.2. Power-On Timings

Parameter	Description	EN25Q32B	MX25L3255D
t _{VSL}	V _{CC} (min) to CS# low	10μs	200μs
t _{PUW}	Time delay to Write instruction	10ms	

5.3. ERASE AND PROGRAM PERFORMANCE

The ERASE and PROGRAM Performance Comparison

Parameter	EN25Q32B		MX25L3255D		Unit
	Typ	Max	Typ	Max	
Page programming time	0.8	5	1.4	5	ms
Sector erase time	0.05	0.3	0.06	0.3	sec
Block erase time	0.2	2	0.7	2	sec
Chip (Bulk) erase time	15	25	25	50	sec



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Revisions List

Revision No	Description	Date
A	Initial Release	2010/8/31