



## **Application Note**

**EON**                      **EN25F16**                      (Version: H)  
**VS.**  
**Numonyx**                **M45PE16**                      (Version: 8)



## 1. INTRODUCTION

The application note introduces how to implement a system design from Numonyx flash M45PE16 to Eon flash EN25F16.

## 2. GENERAL FUNCTION COMPARISON TABLE:

2.1. The following table highlights the major features of these two devices.

Features	EN25F16	M45PE16
Voltage Range	2.7V ~ 3.6V	2.7V ~ 3.6V
Pin to Pin Compatible	NO	NO
SPI Mode	Mode 0 / Mode 3	Mode 0 / Mode 3
SPI Frequency	100MHz (standard mode)	75MHz (standard mode)
Sector Architecture	Uniform <ul style="list-style-type: none"><li>● 512 sectors of 4Kbyte</li><li>● 32 blocks of 64Kbyte</li><li>● Any sector or block can be erased individually.</li></ul>	Uniform <ul style="list-style-type: none"><li>● 32 sectors of 64Kbyte</li><li>● Any sector can be erased individually.</li></ul>
Lockable OTP Security Sector	128 Bytes	No
Hardware write protection of the bottom sector (64 Kbytes)	No	Yes
Block Protection	Yes	No
HOLD# Pin	Yes	No
Reset# Pin	No	Yes
Page Erase	No	Yes
Minimum Endurance Cycle	100K	100K
Package <sup>1</sup> .	8 pins SOP 150mil body width 8 pins SOP 208mil body width 8 contact VDFN 8 pins PDIP <ul style="list-style-type: none"><li>● All Pb-free packages are RoHS compliant</li></ul>	SO8W (MW) 208 mils body width VFQFPN8 (MP) 6 × 5 mm <ul style="list-style-type: none"><li>● All Pb-free packages are RoHS compliant</li></ul>

### Note:

1. Please refer to the datasheet in detail.



## 3. HARDWARE CONSIDERATIONS

### 3.1. I<sub>CC</sub> Comparison

Current	EN25F16	M45PE16	Unit
	Max ( @ 100MHz)	Max ( @ 75MHz)	
Read I <sub>CC3</sub>	25	12	mA
Page Program (PP) I <sub>CC4</sub>	28	15	mA
Sector Erase (SE) I <sub>CC6</sub>	25	15	mA
Standby I <sub>CC1</sub>	20	50	μA

### 3.2. Pins Description

EN25F16		M45PE16	
Pin Name	Function	Pin Name	Function
CLK	Serial Clock Input	C	Serial Clock Input
DI	Serial Data Input	D	Serial Data Input
DO	Serial Data Output	Q	Serial Data Output
CS#	Chip Enable	S#	Chip Enable
WP#	Write Protect	WP#	Write Protect
HOLD#	Hold Input	Reset#	Reset
Vcc	Supply Voltage (2.7-3.6V)	Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground	Vss	Ground

**Note :**

- \* These two devices are not Pin to Pin compatible!



## 4. SOFTWARE CONSIDERATIONS

### 4.1. Manufacturer, Memory Type & Device Identification (M7~M0: manufacture ID, D15~ID0: memory type, ID7~ID0: memory density) comparison.

#### 4.1.1. For EN25F16 : MANUFACTURER/DEVICE ID TABLE

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			14h
90h	1Ch		14h
9Fh	1Ch	3115h	

#### 4.1.2. For M45PE16 : MANUFACTURER/DEVICE ID TABLE

##### Read identification (RDID) data-out sequence

Manufacturer identification	Device identification		UID	
	Memory type	Memory capacity	CFD length	CFD content
20h	40h	15h	10h	16 bytes



## 4.2. Instruction Set Comparison

### 4.2.1. For **EN25F16** : Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0) <sup>(1)</sup>					continuous <sup>(2)</sup>
Write Status Register	01h	S7-S0					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(3)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(4)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(5)		
Enter OTP mode	3Ah						

#### Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until CS# terminates the instruction.
3. The Device ID will repeat continuously until CS# terminates the instruction.
4. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
5. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.



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## 4.2.2. For M45PE16 : Instruction Set

### Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write enable	0000 0110	06h	0	0	0
WRDI	Write disable	0000 0100	04h	0	0	0
RDID	Read identification	1001 1111	9Fh	0	0	1 to 3
RDSR	Read status register	0000 0101	05h	0	0	1 to ∞
READ	Read data bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read data bytes at higher speed	0000 1011	0Bh	3	1	1 to ∞
PW	Page write	0000 1010	0Ah	3	0	1 to 256
PP	Page program	0000 0010	02h	3	0	1 to 256
PE	Page erase	1101 1011	DBh	3	0	0
SE	Sector erase	1101 1000	D8h	3	0	0
DP	Deep power-down	1011 1001	B9h	0	0	0
RDP	Release from deep power-down	1010 1011	ABh	0	0	0

#### Note:

1. The major differences are pointed out by the blue arrows. Please refer to the datasheet in detail.
2. Users must modify the codes for EN25F16!



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## 4.3. Different Block Protection Area

### 4.3.1. For EN25F16 :

Protected Area Sizes Sector Organization Table

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Block 0 to 30	000000h-1EFFFFh	1984KB	Lower 31/32
0	1	0	Block 0 to 29	000000h-1DFFFFh	1920KB	Lower 30/32
0	1	1	Block 0 to 27	000000h-1BFFFFh	1792KB	Lower 28/32
1	0	0	Block 0 to 23	000000h-17FFFFh	1536KB	Lower 24/32
1	0	1	Block 0 to 15	000000h-0FFFFFh	1024KB	Lower 16/32
1	1	0	All	000000h-1FFFFFFh	2048KB	All
1	1	1	All	000000h-1FFFFFFh	2048KB	All

### 4.3.2. For M45PE16 : No such feature!



## 4.4. Different RDSR Bits Definition

The definition of RDSR bits [S7:S2] are different!

### 4.4.1. For EN25F16 :

#### Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	Reserved bits	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit) (Note 3)
1 = status register write disable	1 = OTP sector is protected			(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit				Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

#### Note

1. In OTP mode, SRP bit is served as OTP\_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

### 4.4.2. For M45PE16 :

#### Status register format

b7							b0	
0	0	0	0	0	0	WEL <sup>(1)</sup>	WIP <sup>(1)</sup>	

1. WEL and WIP are volatile read-only bits (WEL is set and reset by specific instructions; WIP is automatically set and reset by the internal logic of the device).



## 4.5. Different One Time Programming Definition

### 4.5.1. For EN25F16 :

#### OTP Sector Address

Sector	Sector Size	Address Range
511	128 byte	1FF000h – 1FF07Fh

**Note:** The OTP sector is mapping to sector 511

### 4.5.2. For M45PE16 : No such feature!



## 5. PERFORMANCE DIFFERENCES

### 5.1. KEY AC PARAMETER PERFORMANCE

Parameter	EN25F16	M45PE16
t <sub>CH</sub> (serial clock high time)	Min @ 4ns	Min @ 9ns
t <sub>CL</sub> (serial clock low time)	Min @ 4ns	Min @ 9ns
t <sub>CLCH</sub> (serial clock rise time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t <sub>CLCL</sub> (serial clock fall time)	Min @ 0.1V / ns	Min @ 0.1V / ns
t <sub>CHSH</sub> (CS# active setup / hold time)	Min@ 5ns	Min @ 5ns
t <sub>SLSL</sub> (CS# high time)	Min @ 100ns	Min @ 100ns
t <sub>DSU</sub> (Data in setup time)	Min @ 2ns	Min @ 2ns
t <sub>DH</sub> (Data in hold time)	Min @ 5ns	Min @ 5ns

### 5.2. Power-On Timings

Parameter	Description	EN25F16	M45PE16
t <sub>VSL</sub>	V <sub>CC</sub> (min) to CS# low	10μs	30μs
t <sub>PUW</sub>	Time delay to Write instruction	10ms	10ms

### 5.3. ERASE AND PROGRAM PERFORMANCE

#### The ERASE and PROGRAM Performance Comparison

Parameter	EN25F16		M45PE16		Unit
	Typ	Max	Typ	Max	
Page programming time	1.3	5	0.8	3	ms
Sector erase time	0.09	0.3	<del> </del>	<del> </del>	sec
Block erase time	0.4	2	1	5	sec
Chip (Bulk) erase time	7	35	<del> </del>	<del> </del>	sec



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## Revisions List

Revision No	Description	Date
A	Initial Release	2010/9/1