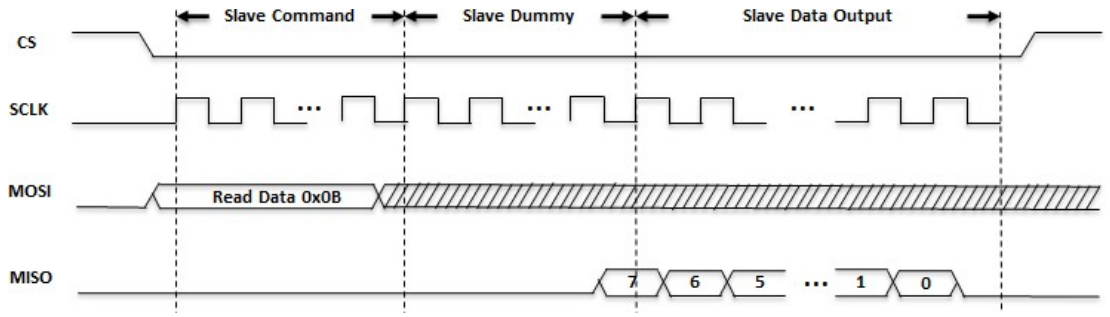

Figure 6.15-4 Timing Diagram of Data-Reading Command

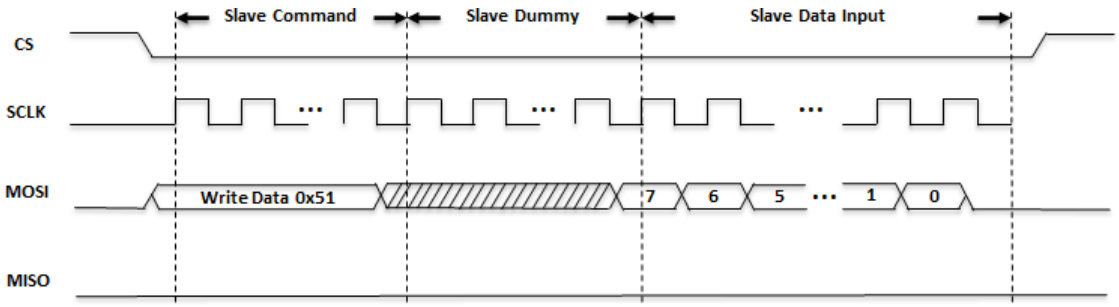

Figure 6.15-5 Timing Diagram of Data-Writing Command

For the user-defined command, the “slave data field” format is defined by the transfer control register (TRNMODE field in TRANSCTRL3 Register). For example, if the transfer mode is {Read Only}, only the data read field will be logged into the data register.

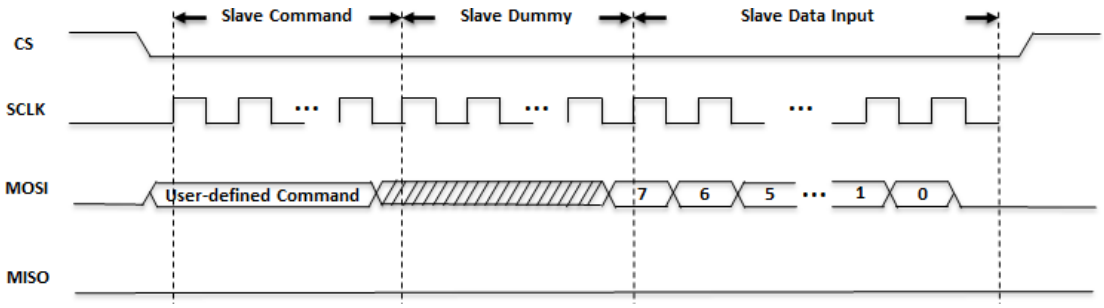

Figure 6.15-6 Timing Diagram of User-defined Command

Note that the user define command provides flexibility for customer to transceiver the data field as compared with read or write data command. Please see section 6.15.2 TRANSCTRL3 Register for more details.

6.15.2 Register Map and Description

Base Address (SPI_BA) : 0xFC00				
Register	**Offset**	**RW**	**Description**	**Reset Value**
TRNFMT0	SPI_BA+0x00	R/W	SPI Transfer Format 0 Register	0x00
TRNFMT1	SPI_BA+0x01	R/W	SPI Transfer Format 1 Register	0x00
TRNCTRL0	SPI_BA+0x02	R/W	SPI Transfer Control 0 Register	0x00
TRNCTRL1	SPI_BA+0x03	R/W	SPI Transfer Control 1 Register	0x00
TRNCTRL2	SPI_BA+0x04	R/W	SPI Transfer Control 2 Register	0x00
TRNCTRL3	SPI_BA+0x05	R/W	SPI Transfer Control 3 Register	0x00
SPICMD	SPI_BA+0x06	R/W	SPI Command Register	0x00
SPIADR0	SPI_BA+0x07	R/W	SPI Address 0 Register	0x00
SPIADR1	SPI_BA+0x08	R/W	SPI Address 1 Register	0x00
SPIADR2	SPI_BA+0x09	R/W	SPI Address 2 Register	0x00
SPIDATA	SPI_BA+0x0A	R/W	SPI Data Register	0x00
SPICTRL0	SPI_BA+0x0B	R/W	SPI Control 0 Register	0x00
SPICTRL1	SPI_BA+0x0C	R/W	SPI Control 1 Register	0x00
SPICTRL2	SPI_BA+0x0D	R/W	SPI Control 2 Register	0x00
SPISTAT0	SPI_BA+0x0E	R/W	SPI Status 0 Register	0x00
SPISTAT1	SPI_BA+0x0F	R/W	SPI Status 1 Register	0x00
SPISTAT2	SPI_BA+0x10	R/W	SPI Status 2 Register	0x00
INTEN	SPI_BA+0x11	R/W	SPI Interrupt Enable Register	0x00
INTSTAT	SPI_BA+0x12	R/W	SPI Interrupt Status Register	0x00
INTFTIM0	SPI_BA+0x13	R/W	SPI Interface Timing 0 Register	0x00
INTFTIM1	SPI_BA+0x14	R/W	SPI Interface Timing 1 Register	0x00
SLVSTAT0	SPI_BA+0x15	R/W	SPI Slave Status 0 Register	0x00
SLVSTAT1	SPI_BA+0x16	R/W	SPI Slave Status 1 Register	0x00
SLVSTAT2	SPI_BA+0x17	R/W	SPI Slave Status 2 Register	0x00
RCVCNT0	SPI_BA+0x18	R/W	SPI Slave Receive Counter 0 Register	0x00
RCVCNT1	SPI_BA+0x19	R/W	SPI Slave Receive Counter 1 Register	0x00
TSMCNT0	SPI_BA+0x1A	R/W	SPI Transmit Counter 0 Register	0x00
TSMCNT1	SPI_BA+0x1B	R/W	SPI Transmit Counter 1 Register	0x00
SPICFG	SPI_BA+0x1C	R/	SPI Configuration Register	0x00

SPI Transfer Format 0 Register

Register	Offset	RW	Description	Reset Value
TRNFMT0	SPI_BA+0x00	R/W	SPI Transfer Format 0 Register	0x00

Bits	Flag	Description
[7:5]	Reserved	**Reserved**.
[4]	MOSIBID	**SPI Bi-directional MOSI in Regular Mode Selection Flag** This bit is set by software, cleared by software. MOSIBID = 0, MOSI is uni-directional signal in regular (single) mode. MOSIBID = 1, MOSI is bi-directional signal in regular (single) mode.
[3]	LSB	**SPI LSB/MSB Bit First Selection Flag** This bit is set by software, cleared by software. LSB = 0, Most significant bit first. LSB = 1, Least significant bit first.
[2]	SLVMODE	**SPI Master/Slave Mode Selection Flag** This bit is set by software, cleared by software. SLVMODE = 0, Master mode. SLVMODE = 1, Slave mode.
[1]	CPOL	**SPI Clock Polarity Phase Flag** This bit is set by software, cleared by software. CPOL = 0, SCLK is LOW in the idle states. CPOL = 1, SCLK is HIGH in the idle states.
[0]	CPHA	**SPI Clock Sampling Phase Flag** This bit is set by software, cleared by software. CPHA = 0, Sampling data at pose-edge SCLK. CPHA = 1, Sampling data at neg-edge SCLK.

SPI Transfer Format 1 Register

Register	Offset	RW	Description	Reset Value
TRNFMT1	SPI_BA+0x01	R/W	SPI Transfer Format 1 Register	0x00

Bits	Flag	Description
[7:6]	ADRLEN	**SPI Address Length Selection Flag** This bit is set by software, cleared by software. ADRLEN = 0, 1-byte address. ADRLEN = 1, 2-byte address. ADRLEN = 2, 3-byte address. ADRLEN = 3, Reserved.
[5]	Reserved	**Reserved**.
[4:0]	DATLEN	**SPI Data Length Selection Flag** This bit is set by software, cleared by software. The actual bit number of a data unit is (DATLEN + 1) : Bit length of data

SPI Transfer Control 0 Register

Register	Offset	RW	Description	Reset Value
TRNCTRL0	SPI_BA+0x02	R/W	SPI Transfer Control 0 Register	0x00

Bits	Flag	Description
[7:0]	RTRNCNT	**SPI Transfer Count for Read Data** This bit is set by software, cleared by software. RTRNCNT indicates the number of units of data to be received from SPI bus and stored to the Date Register. The actual received count is (RTRNCNT+1). RTRNCNT only takes effect when TRNMODE is 0, 2, 3, or 4. The size (bit-width) of a data unit is defined by the DATLEN field of the transfer format register (TRANFMT1). For TRNMODE 0, WTRNCNT must be equal to RTRNCNT.

SPI Transfer Control 235 Register

Register	Offset	RW	Description	Reset Value
TRNCTRL1	SPI_BA+0x03	R/W	SPI Transfer Control 1 Register	0x00

Bits	Flag	Description
[7:4]	WTRNCNT	**SPI Transfer Count for Write Data** This bit is set by software, cleared by software. WTRNCNT indicates the number of units of data to be transmitted to the SPI bus from the Data Register. The actual transfer count is (WrTranCnt+1). WTRNCNT only takes effect when TRNMODE is 0, 1, 3, or 4. The size (bit-width) of a data unit is defined by the DATLEN field of the Transfer Format Register. For TRNMODE 0, WTRNCNT must be equal to RTRNCNT.
[3]	TOKENVU	**SPI Special Token Value Following the Address Phase (Master Mode Only)** This bit is set by software, cleared by software. TOKENVU = 0, Token value = 0x00. TOKENVU = 1, Token value = 0x69.
[2:1]	Reserved	**Reserved**.
[0]	RTRNCNT	**SPI Transfer Count for Read Data** This bit is set by software, cleared by software. RTRNCNT indicates the number of units of data to be received from SPI bus and stored to the Date Register. The actual received count is (RTRNCNT+1). RTRNCNT only takes effect when TRNMODE is 0, 2, 3, or 4. The size (bit-width) of a data unit is defined by the DATLEN field of the transfer format register (TRANFMT1). For TRNMODE 0, WTRNCNT must be equal to RTRNCNT.

SPI Transfer Control 236 Register

Register	Offset	RW	Description	Reset Value
TRNCTRL2	SPI_BA+0x04	R/W	SPI Transfer Control 2 Register	0x00

Bits	Flag	Description
[7:6]	Reserved	**Reserved**.
[5]	TOKENEN	**SPI Special Token Value Enable Flag (Master Mode Only)** This bit is set by software, cleared by software. TOKENEN = 0, One-byte special token disabled. TOKENEN = 1, One-byte special token enabled.
[4:0]	WTRNCNT	**SPI Transfer Count for Write Data** This bit is set by software, cleared by software. WTRNCNT indicates the number of units of data to be transmitted to the SPI bus from the Data Register. The actual transfer count is (WrTranCnt+1). WTRNCNT only takes effect when TRNMODE is 0, 1, 3, or 4. The size (bit-width) of a data unit is defined by the DATLEN field of the Transfer Format Register. For TRNMODE 0, WTRNCNT must be equal to RTRNCNT.

SPI Transfer Control 237 Register

Register	Offset	RW	Description	Reset Value
TRNCTRL3	SPI_BA+0x05	R/W	SPI Transfer Control 3 Register	0x00

Bits	Flag	Description
[7]	Reserved	**Reserved**.
[6]	CMDEN	**SPI Command Phase Enable Flag (Master Mode Only)** This bit is set by software, cleared by software. CMDEN = 0, Command phase disabled. CMDEN = 1, Command phase enabled.
[5]	ADREN	**SPI Address Phase Enable Flag (Master Mode Only)** This bit is set by software, cleared by software. ADREN = 0, Address phase disabled. ADREN = 1, Address phase enabled.
[4]	Reserved	**Reserved**.
[3:0]	TRNMODE	**SPI Transfer Mode Flag** This bit is set by software, cleared by software. TRNMODE = 0, Write and read at the same time. TRNMODE = 1, Write only. TRNMODE = 2, Read only. TRNMODE = 3, Write then read. TRNMODE = 4, Read then write. TRNMODE = 5, Reserved. TRNMODE = 6, Reserved. TRNMODE = 7, None data (must enable CMDEN or ADDREN in master mode). TRNMODE > 8, Reserved.

SPI Command Register

Register	Offset	RW	Description	Reset Value
SPICMD	SPI_BA+0x06	R/W	SPI Command Register	0x00

Bits	Flag	Description
[7:0]	CMD	**SPI Command Register** This bit is set by software, cleared by software. Write operations on this register trigger SPI transfers. This register must be written with a dummy value to start a SPI transfer even when the command phase is not enabled. When the SPI controller is programmed to the slave mode, the command field of the last received SPI transaction is stored in this SPI command register.

SPI Address Register

Register	Offset	RW	Description	Reset Value
SPIADR0	SPI_BA+0x07	R/W	SPI Address 0 Register	0x00

Bits	Flag	Description
[7:0]	SPIADRx, x = 0, 1, 2	**SPI Address x Register, x = 0, 1, 2** This bit is set by software, cleared by software. SPI address.

SPI Data Register

Register	Offset	RW	Description	Reset Value
SPIDATA	SPI_BA+0x0A	R/W	SPI Data Register	0x00

Bits	Flag	Description
[7:0]	SPIDAT	**SPI Data Register** This bit is set by software, cleared by software. For writes, data is enqueued to the TX FIFO. The least significant byte is always transmitted first. For reads, data is read and dequeued from the RX FIFO. The least significant byte is the first received byte. The FIFOs decouple the speed of the SPI transfers and the software's generation/consumption of data. When the TX FIFO is empty, SPI transfers will hold until more data is written to the TX FIFO; when the RX FIFO is full, SPI transfers will hold until there is more room in the RX FIFO. If more data is written to the TX FIFO than the write transfer count (WRTRANCNT), the remaining data will stay in the TX FIFO for the next transfer or until the TX FIFO is reset.

SPI Control 0 Register

Register	Offset	RW	Description	Reset Value
SPICTRL0	SPI_BA+0x0B	R/W	SPI Control 0 Register	0x00

Bits	Flag	Description
[7:3]	Reserved	**Reserved**.
[2]	TFIFORST	**SPI Transmit FIFO Reset Enable Flag** This bit is set by software, cleared by software. TFIFORST = 0, Idle. TFIFORST = 1, Transmit FIFO reset.
[1]	RFIFORST	**SPI Receive FIFO Reset Enable Flag** This bit is set by software, cleared by software. RFIFORST = 0, Idle. RFIFORST = 1, Receive FIFO reset.
[0]	SPIRST	**SPI Reset Enable Flag** This bit is set by software, cleared by hardware. SPIRST = 0, Idle. SPIRST = 1, SPI reset.

SPI Control 242 Register

Register	Offset	RW	Description	Reset Value
SPICTRL1	SPI_BA+0x0C	R/W	SPI Control 1 Register	0x00

Bits	Flag	Description
[7:5]	Reserved	**Reserved**.
[4:0]	RTHRCV	**SPI Receive FIFO Threshold Flag** This bit is set by software, cleared by software. The RXFIFOINT interrupt would be issued for consuming the RX FIFO when the RX data count is more than or equal to the RX FIFO threshold.

SPI Control 243 Register

Register	Offset	RW	Description	Reset Value
SPICTRL2	SPI_BA+0x0D	R/W	SPI Control 2 Register	0x00

Bits	Flag	Description
[7:5]	Reserved	**Reserved**.
[4:0]	TTHTRN	**SPI Transmit FIFO Threshold Flag** This bit is set by software, cleared by software. The TXFIFOINT interrupt would be issued to replenish the TX FIFO when the TX data count is less than or equal to the TX FIFO threshold.

SPI Status 0 Register

Register	Offset	RW	Description	Reset Value
SPISTAT0	SPI_BA+0x0E	R/W	SPI Status 0 Register	0x00

Bits	Flag	Description
[7:1]	Reserved	**Reserved**.
[0]	BUSY	**SPI In Progress Flag** This bit is set by hardware, cleared by hardware. BUSY = 0, Idle. BUSY = 1, SPI direct register programming is in progress.

SPI Status 245 Register

Register	Offset	RW	Description	Reset Value
SPISTAT1	SPI_BA+0x0F	R/W	SPI Status 1 Register	0x00

Bits	Flag	Description
[7]	RFUL	**SPI Receive FIFO Full Flag** This bit is set by hardware, cleared by hardware. RFUL = 0, Receive FIFO not full. RFUL = 1, Receive FIFO full.
[6]	REMP	**SPI Receive FIFO Empty Flag** This bit is set by hardware, cleared by hardware. REMP = 0, Receive FIFO not empty. REMP = 1, Receive FIFO empty.
[5]	Reserved	**Reserved**.
[4:0]	RFIFONUM	**SPI Number of Entries in the Receive FIFO** This bit is set by hardware, cleared by hardware.

SPI Status 246 Register

Register	Offset	RW	Description	Reset Value
SPISTAT2	SPI_BA+0x10	R/W	SPI Status 2 Register	0x00

Bits	Flag	Description
[7]	TFUL	**SPI Transmit FIFO Full Flag** This bit is set by hardware, cleared by hardware. TFUL = 0, Transmit FIFO not full. TFUL = 1, Transmit FIFO full.
[6]	TEMP	**SPI Transmit FIFO Empty Flag** This bit is set by hardware, cleared by hardware. TEMP = 0, Transmit FIFO not empty. TEMP = 1, Transmit FIFO empty.
[5]	Reserved	Reserved.
[4:0]	TFIFONUM	**SPI Number of Entries in the Transmit FIFO** This bit is set by hardware, cleared by hardware.

SPI Interrupt Enable Register

Register	Offset	RW	Description	Reset Value
INTEN	**SPI_BA+0x11**	**R/W**	SPI Interrupt Enable Register	**0x00**

Bits	Flag	Description
[7:6]	Reserved	**Reserved**.
[5]	SLVCMDIEN	**SPI Slave Command Interrupt Enable Flag (Slave Mode Only)** This bit is set by software, cleared by software. SLVCMDIEN = 0, Slave command interrupt disabled. SLVCMDIEN = 1, Slave command interrupt enabled.
[4]	ENDTIEN	**SPI End of Transfer Interrupt Enable Flag** This bit is set by software, cleared by software. ENDTIEN = 0, End of transfer interrupt disabled. ENDTIEN = 1, End of transfer interrupt enabled.
[3]	TFIFOIEN	**SPI Transmit FIFO Interrupt Enable Flag** This bit is set by software, cleared by software. In slave mode, end of read status transaction does not trigger this interrupt TFIFOIEN = 0, Receive FIFO interrupt disabled. TFIFOIEN = 1, Receive FIFO interrupt enabled.
[2]	RFIFOIEN	**SPI Receive FIFO Interrupt Enable Flag** This bit is set by software, cleared by software. RFIFOIEN = 0, Receive FIFO interrupt disabled. RFIFOIEN = 1, Receive FIFO interrupt enabled.
[1]	TFIFOURIEN	**SPI Transmit FIFO Underrun Interrupt Enable Flag (Slave Mode Only)** This bit is set by software, cleared by software. TFIFOURIEN = 0, Receive FIFO underrun interrupt disabled. TFIFOURIEN = 1, Receive FIFO underrun interrupt enabled.
[0]	RFIFOORIEN	**SPI Receive FIFO Overrun Interrupt Enable Flag (Slave Mode Only)** This bit is set by software, cleared by software. RFIFOORIEN = 0, Receive FIFO overrun interrupt disabled. RFIFOORIEN = 1, Receive FIFO overrun interrupt enabled.

SPI Interrupt Status Register

Register	Offset	RW	Description	Reset Value
INTSTAT	SPI_BA+0x12	R/W	SPI Interrupt Status Register	0x00

Bits	Flag	Description
[7:6]	Reserved	**Reserved**.
[5]	SLVCMDINTF	**SPI Slave Command Interrupt Flag (Slave Mode Only)** This bit is set by hardware, cleared by software. SLVCMDINTF = 0, Otherwise. SLVCMDINTF = 1, Slave command interrupt triggered.
[4]	ENDTINTF	**SPI End of Transfer Interrupt Flag** This bit is set by hardware, cleared by software. ENDTINTF = 0, Otherwise. ENDTINTF = 1, End of transfer interrupt triggered.
[3]	TFIFOINTF	**SPI Transmit FIFO Interrupt Flag** This bit is set by hardware, cleared by software. In slave mode, end of read status transaction does not trigger this interrupt TFIFOINTF = 0, Otherwise. TFIFOINTF = 1, Receive FIFO interrupt triggered.
[2]	RFIFOINTF	**SPI Receive FIFO Interrupt Flag** This bit is set by hardware, cleared by software. RFIFOINTF = 0, Otherwise. RFIFOINTF = 1, Receive FIFO interrupt triggered.
[1]	TFIFOURINTF	**SPI Transmit FIFO Underrun Interrupt Flag (Slave Mode Only)** This bit is set by hardware, cleared by software. TFIFOURINTF = 0, Otherwise. TFIFOURINTF = 1, Receive FIFO underrun interrupt triggered.
[0]	RFIFOORINTF	**SPI Receive FIFO Overrun Interrupt Flag (Slave Mode Only)** This bit is set by hardware, cleared by software. RFIFOORINTF = 0, Otherwise. RFIFOORINTF = 1, Receive FIFO overrun interrupt triggered.

SPI Interface Timing 0 Register

Register	Offset	RW	Description	Reset Value
INTFTIM0	SPI_BA+0x13	R/W	SPI Interface Timing 0 Register	0x00

Bits	Flag	Description
[7:0]	SCLKDIV	**SPI Clock Divider Flag** This bit is set by software, cleared by software. SCLK period = ((SCLKDIV+1)×2)×(Period of the SPI clock source) The SCLKDIV value 0xff is a special value which indicates that the SCLK frequency should be the same as the SPI source clock frequency.

SPI Interface Timing 1 Register

Register	Offset	RW	Description	Reset Value
INTFTIM1	SPI_BA+0x14	R/W	SPI Interface Timing 1 Register	0x00

Bits	Flag	Description
[7:6]	Reserved	**Reserved**.
[5:4]	CS2SCLK	**SPI Minimum Time Between Edges of CS and Edges of SCLK** This bit is set by software, cleared by software. The actual duration is (SCLK_Period/2)×(CS2CLK+1)
[3:0]	CSHT	**SPI Minimum Time of CS Stay HIGH** This bit is set by software, cleared by software. The actual duration is (SCLK_Period/2)×(CSHT+1)

SPI Slave Status 0 Register

Register	Offset	RW	Description	Reset Value
SLVSTAT0	SPI_BA+0x15	R/W	SPI Slave Status 0 Register	0x00

Bits	Flag	Description
[7:0]	USERSTAT0	**SPI User Defined Status 0 Flag** This bit is set by software, cleared by software.

The Slave Status Register keeps slave statuses. An SPI master can get these statuses by issuing status-reading commands.

6.17.3 Programming Model (Please refer to “Sample code project”)

Step 1: Set clock pre-scale register by PRESCALE Register

Step 2: Set CAPxLPF, x = 0, 1, 2, 3, of input signal filter in LPFSEL Register

Step 3: Set capture mode by CAPxMODE, x = 0, 1, 2, 3, field of Mode Register

Step 4: Set interrupt enable flag by CAPxEN, x = 0, 1, 2, 3, field of INTEN Register

Step 5: Enable capture channel by CAPxEN, x = 0, 1, 2, 3, field of CAPCTRL Register

Step 6: Wait for Interrupt

Step 7: In capture ISR, read CAPINTF Register for clearing related interrupt flag and read related channel counter value by CAPxCNTL and CAPxCNTH, x = 0, 1, 2, 3 Register